NDIA

TRUSTED MICROELECTRONICS WORKSHOP

Onsite Agenda

February 2, 2017
Lockheed Martin Global Vision Center, Arlington, VA

7:30am – 8:30am	REGISTRATION AND NETWORKING COFFEE
8:30am – 8:35am	WELCOME Mr. James Chew, Group Director, National Security Programs, Cadence Design Systems
8:35am – 8:45am	WORKSHOP INTRODUCTION Dr. Jeremy Muldavin, Deputy Director, Defense Software & Microelectronics Assurance Activities, ODASD (SE)
8:45am – 9:45am	TRUST AND INTEGRITY PERSPECTIVE: 3RD PARTY INTELLECTUAL PROPERTY IN DEFENSE SYSTEMS Moderator: Dr. Brian Cohen, Research Staff Member, Institute for Defense Analyses • Dr. Michael Bear, Technical Director - Systems Engineering, BAE Systems • Mr. Claude Goldsmith, Principal Engineer, Lockheed Martin Corporation • Dr. Thomas Kazior, Senior Principal Fellow, Advanced Microelectronics, Raytheon Company Integrated Defense Systems • Dr. William Phillips, Director, Advanced Technology, Northrop Grumman Corporation • Dr. Warren Snapp, Manager, Solid-State Electronics Technology, The Boeing Company
9:45am – 10:00am	NETWORKING COFFEE BREAK
10:00am – 11:00am	INTELLECTUAL PROPERTY PORTFOLIOS: ELECTRONIC DESIGN AUTOMATION (EDA) PROVIDERS Moderator: Mr. John Hallman, Program Manager, MacAulay-Brown, Inc. • Mr. Dino Bekis, Vice President, Product Marketing, IP Group Cadence Design Systems • Dr. Chi-Foon Chan, President and co-CEO, Synopsys • Mr. Serge Leef, Vice President, New Ventures, Mentor Graphics
11:00am – 11:30am	QUESTIONS & ANSWERS WITH PANEL
11:30am – 12:30pm	LUNCH (provided)
12:30pm – 12:45pm	TRUSTED MICROELECTRONICS JOINT WORKING GROUP Moderator: Dr. Dan Radack, Assistant Director, Institute for Defense Analyses

12:45pm – 1:45pm

TRUSTED MICROELECTRONICS JOINT WORKING GROUP
TEAM 1: FUTURE REQUIREMENTS
Lead: Mr. Charles Adams, Director, Programs, Northrop Grumman Corporation

- Dr. Scott Anderson, Senior Staff Research Scientist, Lockheed Martin Space System
- Dr. Mike Fritze, Senior Fellow, Potomac Institute for Policy Studies
- Mr. Craig Herndon, Director, Critical Technologies Innovation Center, Naval Surface Warfare Center-Crane Division
- Maj Manny Trejo, USAF, Advanced Technology Team Mission Lead, Department of Defense

1:45pm – 2:45pm

TRUSTED MICROELECTRONICS JOINT WORKING GROUP
TEAM 2: TRUSTABLE LEADING EDGE TECHNOLOGY ACCESS
Lead: Mr. Ezra Hall, Executive, GLOBALFOUNDRIES U.S. 2, LLC

- Ms. Anita Balachandra, Senior Vice President, TechVision21
- Mr. James Chew, Group Director, National Security Programs, Cadence Design Systems
- Dr. Brian Cohen, Research Staff Member, Institute for defense Analyses
- Ms. Kelly Hennig, Intellectual Asset Management Lead, Northrop Grumman Corporation
- Mr. Vashisht Sharma, Research Staff Member, Institute for defense Analyses
- Dr. Paul Syers, Research Fellow, Potomac Institute for Policy Studies

2:45pm – 3:00pm

NETWORKING COFFEE BREAK

3:00pm – 4:00pm

TRUSTED MICROELECTRONICS JOINT WORKING GROUP
TEAM 3: TRUSTABLE MICROELECTRONICS STANDARD PRODUCTS
Lead: Mr. Ken Lebo, Systems Engineer, JACOBS CSG

- Mr. Dean Brenner, Product Line Director, Honeywell Aerospace
- Mr. John Hallman, Program Manager, MacAulay-Brown, Inc.
- Mr. Neal Levine, Defense Microelectronics Activity

4:00pm – 5:00pm

TRUSTED MICROELECTRONICS JOINT WORKING GROUP
TEAM 4: NEW METHODS TO INSTILL TRUST IN SEMICONDUCTOR FABRICATION
Lead: Dr. Pat Hays, Chief Engineer, The Boeing Company

- Dr. Todd Bauer, Staff Member, Sandia National Laboratories
- Dr. Greg Creech, Founder, GLC Consulting, LLC
- Mr. Steve McNeil, Principal Engineer, Xilinx
- Mr. John Monk, Director, Semiconductor Foundry Operations, Northrop Grumman Corporation

5:00pm – 5:15pm

WRAP-UP
Dr. Brian Cohen, Research Staff Member, Institute for Defense Analyses

Mr. James Chew, Group Director, National Security Programs, Cadence Design Systems
Mr. James Chew has thirty-two years of strategic development, program management, technology development, and marketing experience in the aerospace, automotive, electronics, and education fields.

Prior to joining Cadence, Mr. Chew served as a propulsion engineer for Boeing Aerospace Company, senior engineer for SPARTA, program manager for Air Force Rocket Propulsion Lab, Director of Rocket Propulsion Technology Plans and Programs for the Air Force Phillips Laboratory, Assistant Staff Specialist for Weapons Technology for the Office of the Secretary of Defense, and the Deputy Director of Air and Surface Weapons Technology for the Office of Naval Research. Mr. Chew also served as Exide's (Nasdaq:XIDE)Vice President for the Military and Specialty Global Business Unit, Product Marketing Consultant for the Dodge Division of Chrysler Corporation, QWIPTECH's Chief Operating Officer, General Motor's American Tuner Program Manager, T/J Technologies Chief Operating Officer, Vice President, Science and Technology, ATK (NYSE: ATK), and SAIC's (NYSE: SAI) Vice President, Space Systems Development Division, L-3 Communications Holdings (NYSE: LLL) Director, Advanced Technologies and Concepts for the Precision Engagement Sector, and Director, Strategic Development, General Atomics.

Mr. Chew earned his Bachelor of Science degree in Mechanical Engineering from the California State Polytechnic University, Pomona and a Master of Science degree in Systems Management from the University of Southern California. Mr. Chew is a graduate of the Stanford Executive Engineering Program and the Defense Systems Management College Advanced Program Management Program.

Dr. Jeremy Muldavin, Deputy Director, Defense Software Microelectronics Assurance Activities, ODASD(SE)
Dr. Jeremy Muldavin received his BSE(95) engineering Physics, MSE(97), PhD(2001) in Electromagnetics from University of Michigan. He spent 15 years with MIT Lincoln Laboratory as a staff, and group leader researching microelectronics, imagers, embedded computing, open architecture, and autonomy. He currently is Director, Defense Software & Microelectronics Assurance Initiative with DASD(SE).

Dr. Brian Cohen, Research Staff Member, Institute for Defense Analyses
Dr. Brian Cohen has been a Research Staff Member in the Information Technology and Systems Division of the Institute for Defense Analyses (IDA) for over 25 years. He received his B.S. EE and Mathematics from Carnegie-Mellon University in 1981, an MS ECE, Systems and Control Theory from University of Massachusetts in 1983 and Ph.D. in Engineering Sciences from Thayer School of Engineering, Dartmouth College in 1988. After graduation, Dr. Cohen held a research professorship at Dartmouth College until 1991 when he joined IDA.

Dr. Cohen has performed a range of studies at IDA, with a focus on

technology and business assessments for national security. Many of these studies have dealt with sensor, electronic and microsystem device technology issues. Recent studies have examined problems with assuring the supply chain for defense systems in the face of increased trends toward off-shore sources.

Dr. Michael Bear, Technical Director – Systems Engineering, BAE Systems
Dr. Michael Bear has been involved in high-reliability electronics for over 30 years from physics-of-failure to ASIC design, and System Engineering. He has been a lead designer on over 30 ASIC/SoCs including a 70GFLOP DSP processor (RADSPEED). Many of the SoCs contained, or were wholly based, on 3rd party IP. He has also co-authored ASIC and FPGA guidelines for mitigation of malicious attacks on FPGA and ASIC, with the Aerospace Corp. He has along co-authored an update to the ASIC and FPGA Circuitware Benchmark for Mission-Critical Systems. He has taught a seminar on ASICs and Security, to key USG engineers and program managers. Dr. Bear is a member of the USAF Scientific Advisory Board and led multiple studies and reviews at the request of the SecAF/CSAF including participating in the study "Cyber Vulnerabilities of Embedded Systems on Air and Space Systems" which has led to follow-on work in the DoD. He has recently been named to a Science and Technology Expert Group in National Academy of Sciences, Engineering and Medicine. He holds a B.S. in Applied Physics from Purdue University and an M.S. in Applied Physics and Ph.D. in

Computational Physics from George Mason University.

Mr. Claude Goldsmith, Principal Engineer, Lockheed Martin Space Systems
Mr. Goldsmith has worked for Lockheed Martin Space Systems focusing on ASIC and FPGA development in various technical and leadership positions since 1986. Prior to his tenure with Lockheed Martin Mr. Goldsmith spent 15 years with Motorola developing CPU and peripheral support ASICs.

In 2014 and 2015 Mr. Goldsmith co-led a cross-industry team with Aerospace Corp under the auspices of the Mission Assurance Improvement Workshop (MAIW). The document that flowed from that MAIW activity was published and released by Aerospace Corp as TOR-2015-02547 "Countermeasures to Mitigate Malicious Attack Risks to ASIC and FPGA Circuit Development". In 2016 Mr. Goldsmith participated as an SME member of a cross- industry review team for Aerospace Corp's drafting of benchmark TR-2016-02265 "ASIC and FPGA Development Benchmark for Mission-Critical Systems.

Presently, Mr. Goldsmith is a Principal Engineer in ASIC & FPGA Development at Lockheed Martin Space Systems; with a focus on advising SSC programs in matters related to the secure development of ASICs and FPGAs internally and by subcontractors. Mr. Goldsmith holds a BSEE from San Jose State University.

Dr. Thomas Kazior, Senior Principal Fellow, Advanced Electronics, Raytheon Integrated Defense Systems
Dr. Thomas Kazior received a Ph.D. from the Department of Material Science and

Engineering at the Massachusetts Institute of Technology. Dr. Kazior is presently a Senior Principal Engineering Fellow at Raytheon Integrated Defense Systems. He is a subject matter expert (SME) in advanced microelectronics, specializing in III-V compound semiconductor technology, advanced packaging and 3D / heterogeneous integration. He has served as principal investigator (PI) for the DARPA COSMOS and DAHI Programs.

Dr. Kazior has authored, coauthored or presented over 100 papers, review articles, conference presentations, invited talks, and a book chapter and holds numerous patents in microelectronics technology. He is a 2001 recipient of Raytheon's Excellence in Technology Award, and the 2012 recipient of Raytheon's Innovation Excellence Award. Dr. Kazior has served as chair of the ITRS (International Technology Roadmap for Semiconductors) subcommittee for III-V device technology and currently sits on the Science Advisory Board for the Semiconductor Research Corporation's (SRC) Semiconductor Technology Advanced Research Network (STARnet) Program.

Dr. William Phillips, Director, Advanced Technology, Northrop Grumman Corporation

Dr. William C. Phillips is the director of Advanced Technology at Northrop Grumman Mission Systems (NGMS) where he leads the development of advanced enabling technologies that support next generation systems. His responsibilities include strategy development, the planning and execution of internally funded R&D projects, and the capture and execution of R&D programs funded by the DoD and intelligence community. Dr. Phillips has profit and loss responsibility for the advanced technology business area that includes a portfolio of programs with a total contract value of over $100M.

In his previous role, he spent three years as the sector product architect for RF systems where he developed technology and system roadmaps for the NGMS enterprise. Dr. Phillips also spent four years as director of Product Technology and Design Integrity in the EM&L organization where he was responsible for product technology strategy and for the engineering management and execution of over $400M of advanced technology business. He previously held several positions in technology leadership and had achieved the position of Consulting Engineer in the System Architecture group.

Dr. Phillips received the B.S. degree in electrical engineering from the University of Maryland in 1987, the M.S. degree in electrical engineering from Johns Hopkins University in 1991, and the Ph.D. degree in electrical engineering from the University of Maryland in 1998.

Dr. Phillips has over 20 years of experience in the development of radar and electronic warfare systems. He has also supported the Department of Defense as a DARPA Program Manager, as a consultant to the Air Force Scientific Advisory Board, and as a member of the White House Semiconductor R&D Roundtable. He holds six U.S. Patents, has seven technical publications, and has received 22 Northrop Grumman Invention Disclosure Awards.

Dr. Warren Snapp, Manager, Solid-State Electronics Technology, The Boeing Company
Dr. Warren Snapp has worked in the area of integrated circuit design, digital and analog electronics design and aerospace electronics subsystems design for thirty five years. He has managed numerous developmental and production electronics programs. He has worked in the design and management of applications in communications, electronic warfare, radar, and infrared sensors. For the last twenty five years he has managed Boeing's corporate center of excellence for integrated circuit design, the Solid-State Electronics Development Center.

His organization has developed over 450 advanced digital, analog, RF/microwave and radiation-hardened integrated circuits and systems in chip and systems in package used in Boeing's commercial, space, and defense products. His organization, which is part of Boeing's central R&D group (Boeing Research and Technology), also performs on a wide range of technolgy development funded by Government research organizations. Current research interests include low-power IC design, radiation-hardening by design, reliability enhancement by design, and RF integrated circuits.

Mr. John Hallman, Program Manager, MacAulay-Brown, Incorporated
Mr. John Hallman has over 20 years of experience in the Defense industry involving research, development, and process definition of microelectronic components and their implementation in government systems. He is currently the Program Manager for Trust Solutions at MacAulay-Brown Incorporated (MacB) in the Secure Computing and Communications Division. His responsibilities include leadership roles in DARPA research programs for Microelectronic Trust and transforming research ideas into new innovative engineering service solutions in the areas of FPGA Trust, assurance and obsolescence. In addition, Mr. Hallman contributes in the NDIA Trusted Microelectronics Joint Working Group and leads an effort for Netlist Assurance under the SAE G19 Tampered Working Group.

In addition to his work at MacB, Mr. Hallman spent 11 years as a Hardware Engineer designing and implementing complex digital ASICs and FPGAs in the electronic hardware of government communication systems. John has a BS in Electrical Engineering from Florida State University.

Mr. Dino Bekis, Vice President, Product Marketing, IP Group Cadence Design Systems
Mr. Dino Bekis serves as the vice president of marketing for the IP Group in Cadence. In this role, he is responsible for product marketing, business development, collateral and program management for Cadence's entire commercial IP product portfolio, including the broad spectrum of Tensilica DSPs, high-speed analog & mixed signal products, and complete subsystem solutions for a variety of protocols including memory, storage, Ethernet, display, and peripheral interfaces.

Prior to joining Cadence in 2016, Mr. Bekis worked at Broadcom Ltd., where he lead the Passive Optical Networking Customer Premise Equipment (PON CPE) business

in Broadcom's Broadband Communication Access division. In this role, he managed marketing and business development with Operators and OEMs, and directed the engineering efforts for the development of complete platform solutions including gateway SoCs, wireless connectivity subsystems, hardware, software and firmware. Prior to the merger of Broadcom Corp. with Avago, Mr. Bekis spent 9 years at Broadcom Corporation in a variety of roles including vice president of marketing for the wireless connectivity division, leading the marketing and engineering of WiFi, Bluetooth, GPS, NFC and a variety of ASIC solutions for the mobile market. Through his efforts, the company launched several new lines of business that enabled the group to become the largest business unit in the company.

Throughout his 25+ years of enterprise, networking and consumer market experience, he has launched a variety of technologies with Broadcom, PMC-Sierra and IBM including residential gateways, network attached storage (NAS) devices, VoIP platforms, Metro Ethernet solutions and a variety of System-on-Chip processors and software solutions. At the forefront of several commercial technology introductions from low-power WiFi, NFC, 60GHz, and advanced metro-optical architectures, Mr. Bekis also was part of the small core leadership team at IBM that led the Microelectronics Division to become one of the largest merchant semiconductor players.

He earned a Bachelor of Science in Computer & Systems Engineering and a Master's of Science in Electrical Engineering from Rensselaer Polytechnic Institute and an MBA from Marist College.

Dr. Chi-Foon Chan, President and co-CEO, Synopsis

As Synopsys' co-CEO, Dr. Chi-Foon Chan shares responsibility for crafting vision and strategy, leading the company, and ensuring execution excellence in support of our customers' success. As the company's President and COO, a role Dr. Chan held for 14 years prior to his 2012 appointment to President and co-CEO, he guided internal operations and worldwide field organizations.

Dr. Chan joined Synopsys in 1990 as Vice President of Applications and Services where he helped build the Technical Field organization. He has sponsored several key initiatives such as entering the IP market, and personally facilitated key acquisitions such as Avant!, Virage Logic, Magma Design Automation and SpringSoft. In 2014, he led Synopsys' entry into the software testing market with the acquisition of Coverity, and the software security market with the acquisition of Codenomicon.

Prior to Synopsys, Dr. Chan contributed to industry leading companies like NEC Corporation, where he was General Manager of the microprocessor group, responsible for marketing all NEC chip devices in North America. Prior to NEC, Dr. Chan was an engineering manager at Intel Corporation. Dr. Chan holds an M.S. and a Ph.D. in Computer Engineering from Case Western Reserve University; and a B.S. in Electrical Engineering from Rutgers University.

Mr. Serge Leef, Vice President, New Ventures, Mentor Graphics

Mr. Serge Leef is the Vice President of New Ventures Division. He is responsible for identifying and developing product

opportunities for EDA in adjacent, systems-oriented markets. In addition to early stage programs, Mr. Leef leads on-going early stage businesses focused on markets where system-level design plays a pivotal role: cyber-physical system design, systems engineering, design data management, cloud-based electronic design, IoT infrastructure, and hardware cybersecurity.

Mr. Leef has served on the Electrical and Computer Engineering Strategic Advisory Board at North Carolina State University and was a member of Oregon's Engineering and Technology Industry Council (ETIC) which advises the state's public university system on engineering, computer science and technology programs.

Prior to joining Mentor Graphics in 1990, he was responsible for design automation at Silicon Graphics, where his team created revolutionary high-speed simulation tools to enable design of high speed 3D graphics chips that defined state-of-the-art in visualization, imaging, gaming and special effects for a decade. Before 1987, Mr. Leef managed a CAE/CAD organization at Microchip Inc. From 1982 to 1987 Serge worked at Intel Corp. developing functional and physical design and verification tools for major 8- and 16-bit microcontroller and microprocessor programs. Mr. Leef holds a BS in Electrical Engineering and MS in Computer Science from Arizona State University.

Dr. Dan Radack, Assistant Director, Institute for Defense Analyses
Dr. Daniel J. Radack is Assistant Director with the Institute for Defense Analyses (IDA) where he leads projects related to semiconductors and packaging, industrial capabilities, and defense applications.

Dr. Radack was previously with the Defense Advanced Research Projects Agency, Microsystems Technology Office (DARPA/MTO), as a Program Manager for high performance microelectronics and related technologies.

Prior to that, Dr. Radack was with SAIC working on defense electronics programs and for NIST in the Semiconductor Electronics Division where he developed dynamic test circuits and test structures for VLSI processes. He received the B.S. (1983), M.S. (1985), and Ph.D. (1989) in Electrical Engineering from the University of Maryland, College Park. He is a Fellow of the IEEE.

Mr. Charles Adams, Director of Programs, Northrop Grumman Mission Systems
Mr. Charles Adams is director of Programs for the Northrop Grumman Mission Systems sector's Semiconductor Foundry in Linthicum, Maryland. In this role, his primary focus is to develop discriminating semiconductor technology for DoD products. Prior to his current role, Mr. Adams has spent his career in the development of space systems and advanced sensor technologies for multiple customers, and specializes in device level technologies and EO and RF sensor systems.

He earned a bachelor's degree in electrical engineering from Georgia Tech and a master's degree in systems engineering from the University of Maryland, Baltimore County. Outside of work, his passion is

developing the future generations of scientists and engineers to create innovative solutions for tomorrow. He currently resides in Perry Hall, Maryland with his wife and two young children.

Dr. Scott Anderson, Senior Staff Research Scientist, Lockheed Martin Space Systems
Dr. Scott Anderson is a Sr. Staff Research Scientist with Lockheed Martin Space Systems Company's Advanced Technology Center. He has a Ph.D. in Nuclear Engineering from the University of Michigan with an emphasis in low and medium temperature plasmas and plasmas diagnostics. Prior to joining LM, Dr. Anderson was a key account technologist for Applied Materials in the areas of semiconductor process and equipment development for advanced dielectrics, photo masks processing, and nanomaterials.

With Lockheed Martin, his focus is in the areas of advanced electronics development for space applications, advanced electronics system integration, development of adjacent technology strategies and trusted foundry liaison. Dr. Anderson also supports Lockheed Martin's corporate initiatives in cross business area advanced electronics strategy development.

Dr. Michael Fritze, Senior Fellow, Potomac Institute for Policy Studies
Dr. Michael Fritze leads the Microelectronics Policy efforts at the Potomac Institute which he joined in April of 2015. His current focus is on innovative approaches to secure assured trusted access for USG Microelectronics needs. A pressing problem in the wake of the recent IBM Microelectronics sale and the globalization of this critical Industry.

Prior to PIPs, Dr. Fritze was the Director of the Disruptive Electronics Division at the USC Information Sciences Institute (2010-2015). He also held a Research Professor appointment in the USC Ming Hsieh Department of Electrical Engineering (Electrophysics). He was a Program Manager at the DARPA Microsystems Technology Office (MTO) from 2006-2010 with a broad Microelectronics portfolio including 3DIC, Low Power Electronics, Rad-hard electronics, Carbon electronics, Si-RF electronics, Low volume manufacturing and foundry access issues. Prior to joining DARPA, Dr. Fritze was a staff member from 1995-2006 at MIT Lincoln Laboratory in Lexington, Massachusetts, where he worked on fully-depleted silicon on insulator (FDSOI) technology development with an emphasis on fabrication methods & novel devices.

Dr. Fritze received a Ph.D. in Physics from Brown University in 1994 and a B.S. in Physics in 1984 from Lehigh University. He is a recipient of the Office of the Secretary of Defense Medal for Exceptional Public Service awarded in 2010. He is a Senior Member of the IEEE and is active on the program committee of the GOMAC conference. Dr. Fritze has published over 75 papers and articles in professional journals and holds several U.S. Patents.

Mr. Craig Herndon, Director, Critical Technologies Innovation Center, Naval Surface Warfare Center – Crane Division

Mr. Craig Herndon is a 1987 graduate of Purdue University, where he received his Bachelor of Science degree in Electrical Engineering. Mr. Herndon has also received his Defense Acquisition Workforce Improvement Act Level II certification in Systems Planning, Research, Development, and Engineering (1997) and level III certification in Program Management (2006). Mr. Herndon began his civil service career at Naval Surface Warfare Center, Crane Division (NSWC Crane) as a Cooperative Engineering Education Student in 1983. Mr. Herndon's early assignments included multiple engineering roles in Rocket Warheads & Fuzes, Special Purpose Munitions development for the Naval Special Warfare community, and Conventional Surface Warfare Ammunition acquisition.

Mr. Herndon also served as Commodity Manager for Navy Gun Ammunition in the Navy's 2T Cog Conventional Ammunition and Night Vision Program Office (PEO-IWS3C/PM4), where his responsibilities included overall planning, direction, and success of Other Ship Gun Ammunition (OSGA), Intermediate Caliber ammunition, and Major Caliber gun ammunition development and acquisition programs. In 2010, Mr. Herndon transitioned to his present position as Director of the Critical Technologies Innovation Center at NSWC Crane. In this role, Mr. Herndon is focused on providing national leadership to advance technologies for Interconnects, Trusted Electronics, Power & Energy, Technology Protection, and RF devices. In 2012, Mr. Herndon took on additional duties to serve as Program Manager in NSWC Crane's role as the DoD's Executive Agent Technical Lead for Printed Circuit Board & Interconnect Technology, ensuring access to manufacturing capabilities and technical expertise necessary to meet future military requirements.

Mr. Herndon is a member of the American Society of Naval Engineers and the Defense Acquisition Professional Community. Mr. Herndon also serves on the Greene County (Indiana) Project Lead The Way Advisory Board where he has served as past Vice President and past President and volunteers his time in the Linton-Stockton School District to assist with the Sea-Perch Underwater Robotics Program.

Maj Manuel Trejo Jr., USAF, Advanced Technology Team Mission Lead, Department of Defense

Maj Manuel Trejo is the Mission Lead for the Advanced Technology Team under the Hardware Requirements Office, formerly the Trusted Access Program Office (TAPO) at Fort Meade, Maryland. He received his B.S. in Electrical Engineering from The University of Texas at San Antonio in 2006 and a M.S. in Electrical Engineering from Wright State University in 2010. After graduation from UTSA, he received a commission as an officer in the United States Air Force and was assigned to the Air Force Research Lab's Sensors Directorate in Dayton, Ohio as an Electronics Devices Research Engineer.

After five years of extensive work in device fabrication, materials characterization and testing of Gallium Nitride-based HEMTs for high frequency/high power

applications, he was reassigned overseas supporting the Intelligence Community as a field engineer for sensitive systems. Since 2014, Major Trejo has been assigned to Fort Meade, Maryland where he has served as a Microelectronics Program Manager and currently leads a team of engineers exploring emerging and innovative microelectronics technologies for national security applications.

Mr. Ezra Hall, Executive, GLOBALFOUNDRIES U.S. 2 LLC
Mr. Ezra Hall is an executive at GLOBALFOUNDRIES with 26 years of electrical engineering experience and 15 years of project management leadership. Mr. Hall's previous employment includes over 20 years at IBM. Mr. Hall manages complex semiconductor related projects and programs for commercial and government customers, spanning small to large engagements across technical, business, and project management leadership roles, with specialization in bridging across these disciplines.

In the process of joining GLOBALFOUNDRIES, Mr. Hall successfully led a major divestiture work-stream for the transition from IBM Microelectronics to GLOBALFOUNDRIES. This result was achieved through leading team members across multiple companies/divisions and closing complex negotiations between industry and the government. Mr. Hall applies a high degree of innovation in managing projects and solving challenges with a results oriented approach.

Ms. Anita Balachandra, Senior Vice President, Techvision21
Ms. Anita Balachandra works with small and large technology businesses to identify and pursue Federal partners. Prior to TechVision21, Ms. Balachandra worked for the Maryland Technology Development Corporation (TEDCO), working closely with Federal laboratories to showcase their capabilities and technology licensing opportunities. She also worked with small technology-based businesses, including start-ups, to identify appropriate Federal laboratory resources, research collaborators, state and Federal funding sources and business assistance, such as incubator space. Ms. Balachandra began her career at the U.S. Department of Commerce, Office of Technology Policy.

Ms. Kelly Hennig, Intellectual Asset Management Lead, Northrop Grumman Aerospace Systems
Ms. Kelly Hennig leads the Intellectual Asset Management organization for Northrop Grumman's Aerospace Systems sector, a portfolio encompassing semiconductors, communication systems, autonomous systems, and air and space vehicles. Ms. Hennig is intimately involved in the company's technology strategy process and is currently developing the CMOS & Microelectronics technology strategy for NGAS. Prior to her current role, Ms. Hennig managed various research and development programs for the company. Ms. Hennig received her B.S. EE from Rutgers University, and M.S. EE from University of Michigan and holds 8 Patents and has received multiple technology awards in the area of microelectronics.

Northrop Grumman is a $30 billion global defense and technology company whose 120,000 employees provide innovative systems, products and solutions in information and services, electronics, aerospace and shipbuilding and commercial customers worldwide.

Mr. Vashisht Sharma, Research Staff Member, Institute for Defense Analyses
Mr. Sharma, currently a Research Staff Member at IDA, has been in Semiconductor Microelectronics R&D and Manufacturing for the last 40+ years. Prior to joining IDA, he has worked at Microelectronics Development Laboratory/ NSA (3years); Retired as a Senior engineer from IBM and had worked in Engineering and management capacities at IBM (26 years+) E. Fishkill, Burlington and Manassas. His work experience includes technology and process/tool developments in areas starting from Si wafer thru FEOL and BEOL and Packaging for CMOS and Bipolar devices.

His activities at IDA are in Research& Assessments of defense microelectronics advanced technology and materials; advance packaging and interconnect technologies; microelectronics strategy for Trusted Foundry; Trust and Vulnerability analysis of IC supply Chain /SCRM and evaluation of program protection plans for defense systems for ensuring Trusted components. With IDA team, he supports DOD / Agency programs in advance microelectronics areas.

Mr. Sharma received his B.Sc. in Materials Engineering from IIT (BHUIndia), M.Sc. In Materials Science (Univ. of Wisconsin) and MBA (Univ. of Vermont). Among other awards, he is also a recipient of IBM Components (GTD) President's Award. He is a senior member of IEEE.

Dr. Paul Syers, Research Fellow, Potomac Institute for Policy Studies
Joining the Potomac Institute in September 2015, Dr. Syers is a Research Fellow and member of the Center for Revolutionary Scientific Thought (CReST). His current projects focus on policies increasing the Government's ability to access secure and Trusted microelectronics as well as policies addressing arising issues related to machine learning and AI.

Dr. Syers received his Ph.D. in Physics from the University of Maryland, having researched methods for improving the material quality of topological insulators. Prior to that, Dr. Syers received a B.S. in Physics from Emory University and an M.Phil. from the University of Cambridge for research on high temperature superconductors.

Mr. Kenneth Lebo, Systems Engineer, JACOBS CSG
Mr. Kenneth Lebo is a systems engineer with Jacobs Cyber Security Group (CSG) assigned to the Pentagon where he has been supporting the Trusted Foundry Program for over nine years. Prior to his role as a government contractor he was a civilian government employee of the National Security Agency for 20 years. Mr. Lebo worked in the Information Assurance Directorate in various roles related to the manufacture of cryptographic equipment.

Mr. Dean Brenner, Product Line Director, Honeywell Aerospace
Mr. Dean Brenner is the Product Line Director of Space Navigation and Electronics at Honeywell Aerospace, a position he has held since May 2011.

Mr. Brenner is responsible for the product line business strategy, roadmap, investment plans, and overall product line health for Space Navigation & Electronics products. He's product line portfolio includes Inertial Guidance Systems, Electronics Systems, and the Trusted, RadHard Microelectronics foundry supporting Satellite, Strategic Missiles, Human Space, and Launch Vehicles market areas.

Prior to being the Director of Space Nav and Electronics Product Line, Mr. Brenner was the Business Development Director of Military Space and National Programs, a role that started in November 2006. Mr. Brenner joined Honeywell in 1997 as a Principal Staff Systems Engineer in the Defense and Space Systems business. His role covered advanced systems flight development programs including Space Based Infrared Systems (SBIRS) High and SBIRS Low (STSS). Mr. Brenner was also Program Manager of Honeywell Satellite Programs, Defense and Space where he established new product entries for Honeywell in the areas of high-performance military and NASA electronic space systems.

Mr. Brenner holds a Master's of Science in Electrical Engineering from the University of Florida. He lives in Largo, FL with his wife Kathy and their two children, Brooke and Craig.

Mr. Neal Levine, Defense Microelectronics Activity
Mr. Neal Levine has been working in the areas of design, fabrication and yield enhancement (including of secure fabrication at both commercial and government facilities) since 1980. He has supported the Trust program and its accreditation activities since its inception. He received his BS Electrical Engineering (1973) and his MS Solid State Physics (1976) both from The Ohio State University.

Dr. Pat Hays, Chief Engineer, The Boeing Company
Dr. Pat Hays is Chief Engineer at Boeing Secure Computing Solutions where he focuses on the business planning and technology roadmap for Boeing's tamper-resistant secure processors. He joined Boeing in 2013 with its acquisition of CPU Tech. As Vice President at CPU Tech, Dr. Hays established the semiconductor business unit and managed the development of the secure processor, acquired by Boeing.

Throughout his semiconductor career Dr. Hays has specialized in developing new programmable architectures to meet the challenges of new algorithms, especially for telecommunications, video coding and other real-time applications.

Dr. Hays's career highlights include his work at Bell Labs as principal architect of some of industry's first programmable digital signal processors. He was co-founder and CTO of Lexra and just prior to his current work on secure processors, Dr. Hays was Vice President of Engineering at MIPS Technologies.

Dr. Hays is a past recipient of the International Solid State Circuits Conference (ISSCC) Best Paper Award. His chip designs have shipped hundreds of millions of units. Dr. Hays received his undergraduate degree from Harvard and his PhD from MIT, both in Physics.

Dr. Todd Bauer, Staff Member, Sandia National Laboratories
Dr. Todd Bauer is a staff member at Sandia National Laboratories in the MESAFab Operations organization. His sustaining responsibilities are in plasma etch as a tool and process owner, and he is a process integrator for a variety of microsystems. Dr. Bauer also owns Sandia's Trusted fabrication flow and executes research toward trustworthy hardware. He received his Ph.D. in Chemical and Nuclear Engineering in 2001.

Dr. Greg Creech, Founder GLC Consulting, LLC
Dr. Greg Creech recently moved to the Huntsville, Alabama area and founded an independent consulting company, GLC Consulting, LLC (GLC2). He has over 30 years of experience in the Computer-Aided Design of analog, digital, and mixed-signal integrated circuits (IC), advanced sensor component development, and IC hardware assurance (Trusted Microelectronics). He separated from The Ohio State University, ElectroScience Laboratory (OSU-ESL) at the end of December in 2016.
Dr. Creech joined OSU-ESL as the Assistant Director in 2012 after retiring from the Air Force Research Laboratory. While at ESL he successfully led several new research activities while creating new business alliances with government and industry focusing on trusted microelectronics, advanced sensors and communication technologies. Prior to joining the ESL, he worked for the Air Force Research Laboratory, Sensors Directorate (AFRL/RY) for more than 27 years. He was the principle components strategist for the Aerospace Components and Subsystems Division (AFRL/RYD) where he established a research portfolio to develop technology to detect and/or prevent counterfeit and/or malicious circuits from being inserted into the microelectronics supply chain.

Mr. Steven McNeil, Principal Engineer, Xilinx, Inc.
Mr. Steven McNeil is a Principal Engineer at Xilinx with nearly 25 years of semiconductor experience ranging from manufacturing to circuit design to customer applications. Mr. McNeil is the technical lead for Xilinx's Trust and Information Assurance programs and a core member of Xilinx's Security Center of Excellence based in Albuquerque, NM. Mr. McNeil currently manages an Engineering team in the Market Segment Engineering Division servicing Aerospace and Defense, Industrial, and Automotive markets.

Prior to his work in these markets, Mr. McNeil held positions in Product Engineering and IC Design working on CPLDs and FPGAs. Prior to Xilinx, Mr. McNeil worked at Philips Semiconductors in both Process Engineering and Device Failure Analysis. Mr. McNeil received a BS in Electrical Engineering from the University of New Mexico in 1995.

Mr. John Monk, Director, Semiconductor Foundry Operations, Northrop Grumman Corporation
Mr. John Monk is the Director of Northrop Grumman's Advanced Technology Laboratories Semiconductor Foundry Operations which provides internal, integrated circuit capability for Northrop Grumman Systems. He is responsible for oversight of all semiconductor manufacturing, engineering, development, and facility activities that result in annual product deliveries of ~250,000 production parts per year. Process technologies include mixed signal CMOS at several different technology nodes, high voltage BiCMOS, SiGe and SiC Power Transistors, GaAs and GaN MMIC's, plus other discriminating processes for internal systems.

Mr. Monk graduated from the Johns Hopkins University in 1981 with a BS degree in Electrical Engineering. Prior to joining Northrop Grumman he was General Manager for Infinera Corporation's Planar Lightwave Circuits Group. Mr. Monk also spent twelve years at National Semiconductor Corporation where he was the Director of Manufacturing Operations for a semiconductor facility that supported Department of Defense requirements. After graduation and prior to joining National Semiconductor Mr. Monk was an integration engineer at Westinghouse Corporation with a background in rad-hard CMOS and BiCMOS technologies.