NDIA

NDIA Trusted Microelectronics Joint Working Group

Team 2:
Trustable Leading Edge Technology Access

JWG2 Team Members

	Name	Organization	Email
1	Brett Attaway	AIM Photonics Institute	BAttaway@sunypoly.edu
2	Anita Balachandra	TechVision21	abalachandra@techvision21.com
3	Gerry Borsuk	NRL	gerald.borsuk@nrl.navy.mil
4	Brad Botwin	Department of Commerce	brad.botwin@bis.doc.gov
5	James Chew	Cadence	jsbchew@cadence.com
6	Brian Cohen	IDA	bcohen@ida.org
7	Mark Crawford	Department of Commerce	Mark.Crawford@bis.doc.gov
8	Gerry Etzold	Etzold Technology Consulting	etztechcon@gmail.com
9	Aman Gahoonia	DMEA	aman.gahoonia@dmea.osd.mil
10	David Gottfried	Alfred University	gottfried@alfred.edu
11	Ezra Hall (Team Leader)	GLOBALFOUNDRIES	ezra.hall@globalfoundries.com
12	Adam Hauch	DSS	adam.hauch@dss.mil
13	Kelly Hennig	Northrop Grumman	Kelly.Hennig@ngc.com
14	Dan Holladay	University of Central Florida	dan.holladay@ucf.edu
15	Michael James	IBM GBS	Jamm@us.ibm.com
16	Taffy Kingscott	IBM	tking@us.ibm.com
17	Neal Levine	DMEA	neal.levine@dmea.osd.mil
18	Erika Maynard	Department of Commerce	Erika.Maynard@bis.doc.gov
19	Jeremy Muldavin	DASD(SE) Microelectronics Assurance	jeremy.b.muldavin.civ@mail.mil
20	Doug Palmer	Booz Allen Hamilton	Palmer_Doug@bah.com
21	David Pentrack	DMEA	david.pentrack@dmea.osd.mil
22	Christine Rink	The Aerospace Corporation	christine.m.rink@aero.org
23	Neil Schumacher	IBM GBS	neilw@us.ibm.com
24	Vashisht Sharma	Institute for Defense Analyses	vsharma@ida.org
25	Paul Syers	Potomac Institute for Policy Studies	psyers@potomacinstitute.org
26	John Verwey	Department of Commerce	john.verwey@bis.doc.gov
27	Pete Wheatley	DoD	fpwheat@nsa.gov

https://goo.gl/nRWmPk

Goals for 2/2 NDIA Meeting

- **Share preliminary working group findings**
- **Gather input, including direction for focus and further development, for the final work product**
- **Collaborate with other working groups across domains**
- **Deliverables:**
  - Presentation at GOMAC, March 20, 2017, Reno, NV
  - White Paper, March 31, 2017

https://goo.gl/nRWmPk

JWG2 Questions and Sub-Teams

(1)Consequences: What are the potential consequences of the Chinese Government's substantial global semiconductor investments to the U.S. commercial and defense microelectronics industrial base?

(2)Impacts: What are the economic and national security implications of losing access to reliable U.S. and non-U.S. foundries, manufactured components, equipment, intellectual property, and know how, for both commercial and Trusted handling levels?

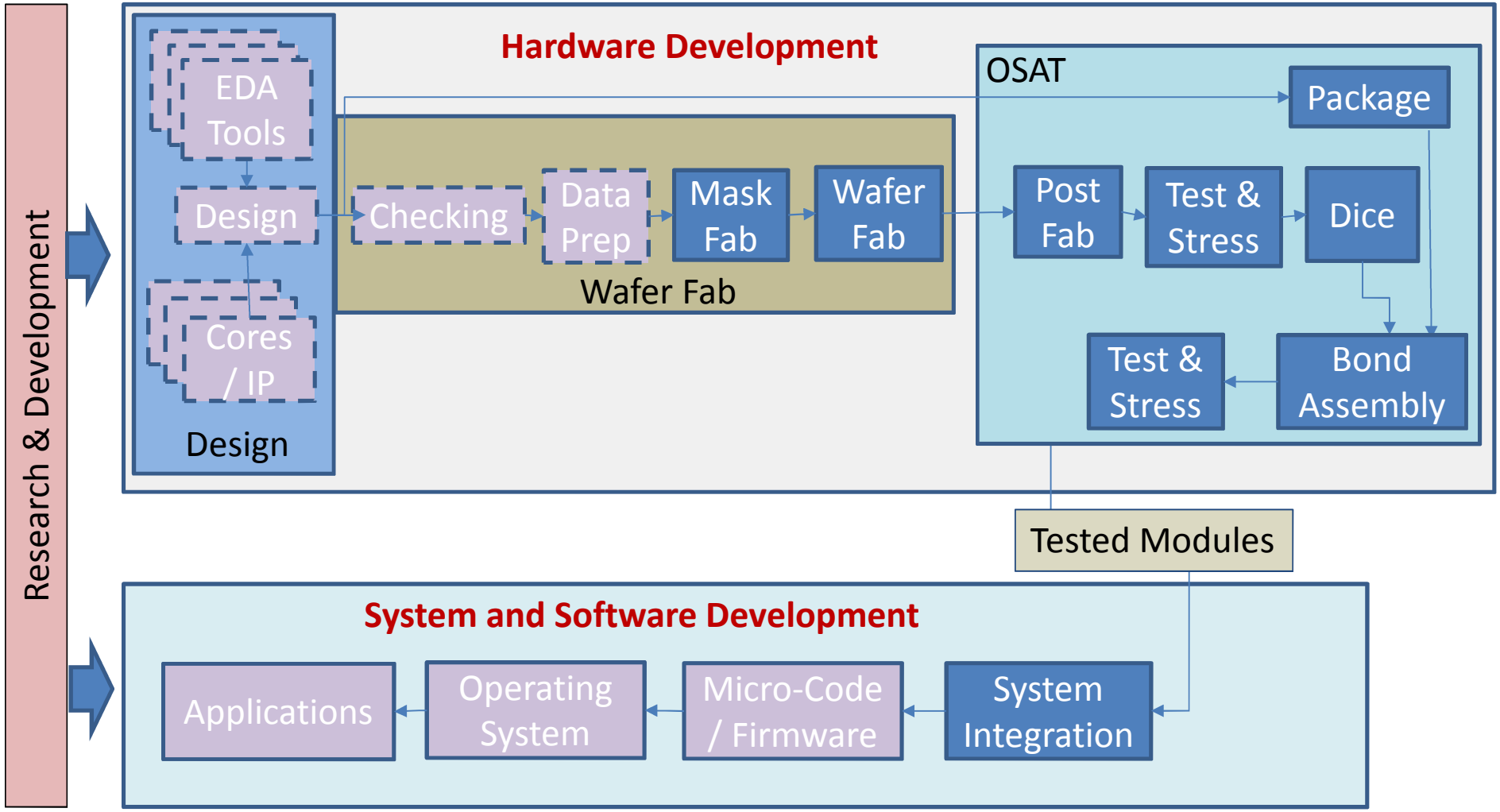
(3)Actions: What actions (Industry and USG) could be taken to stabilize and sustain the U.S. defense microelectronics industrial base?

Our Sub-Teams:

- Acquisition Reform
- Aggregation Models
- Trust Models
- 21st Century SoCs
- End-to-End Education
- National Policy and Public-Private Partnerships

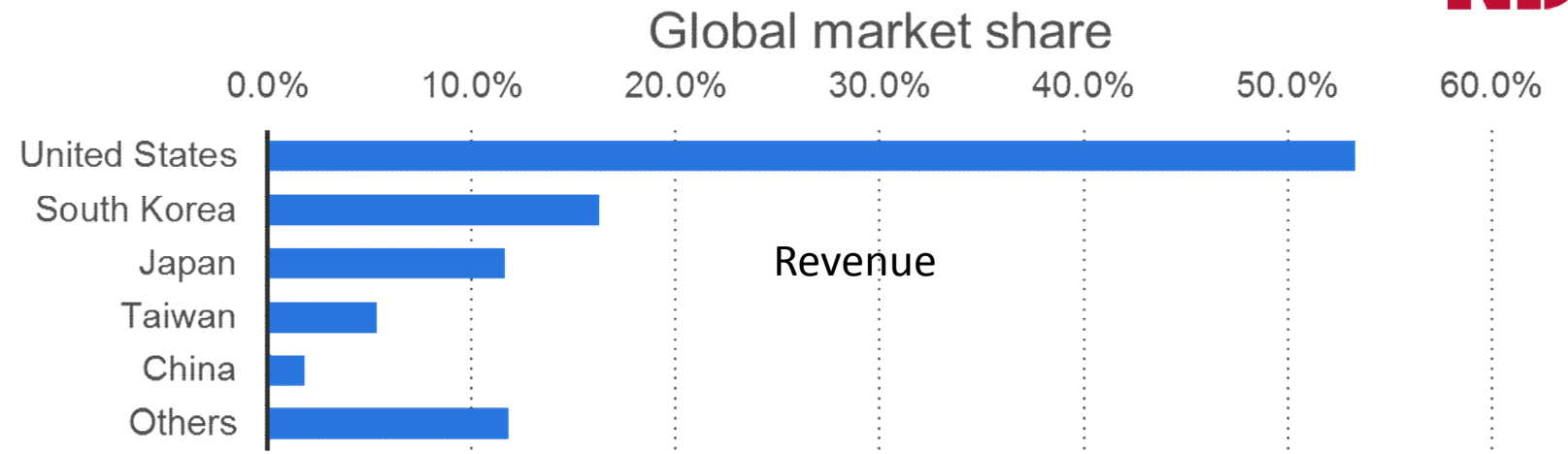
https://goo.gl/nRWmPk

End to End (E2E) Workflow



https://goo.gl/nRWmPk

Global Market State of Play

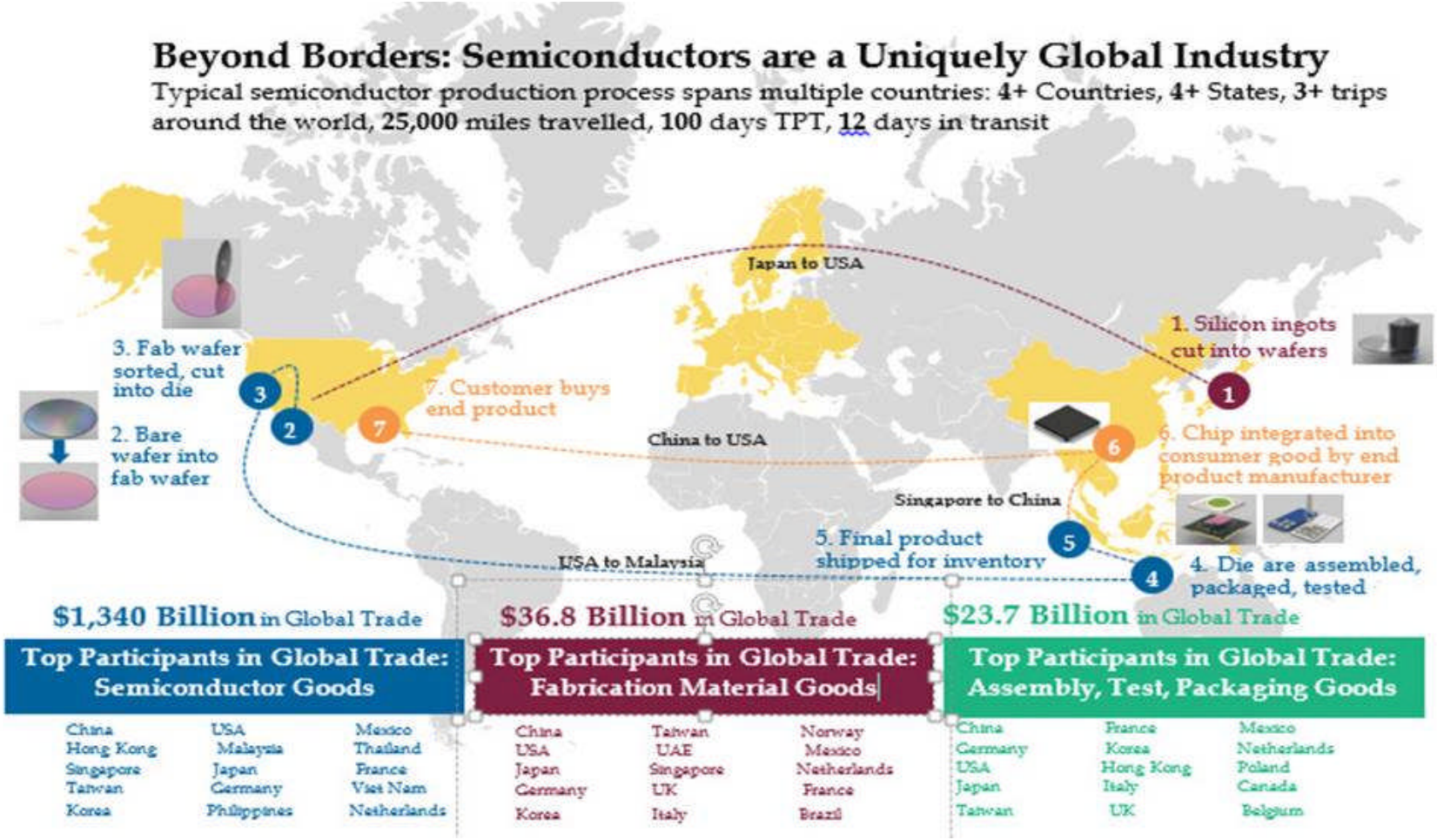


Note: Worldwide; 2014

Source: IHS; Website (businesskorea.co.kr); ID 510374

- US is global market leader (revenue)
  - Accounted for ½ of the global semiconductor sales over past 20 years
  - US companies earn the largest share of revenues in most critical areas
  - A little over 20 percent of global planned front end semiconductor fabs in 2017-2018 are owned by U.S. firms.
- US is losing domestic fab capacity
  - Share of world wide fab capacity in US fell to about 13% in 2015, down from 30% in 1990, and 42% in 1980
- Major Consolidation, Globalization:
  - Companies offering leading edge technology has recently consolidated to 4 companies.
    - Intel (U.S.), GLOBALFOUNDRIES (Abu Dhabi), Samsung (Korea), TSMC (Taiwan)
    - Driven by drastically increasing costs of production for advanced nodes
    - Increases the volumes major producers must sell to obtain return on investment (ROI)
  - Major semiconductor companies have increasing presence on multiple continents.

Commercial Foundation



http://www.semiconductors.org/semiconductors/the_global_semiconductor_value_chain/

https://goo.gl/nRWmPk

Analogous Situations

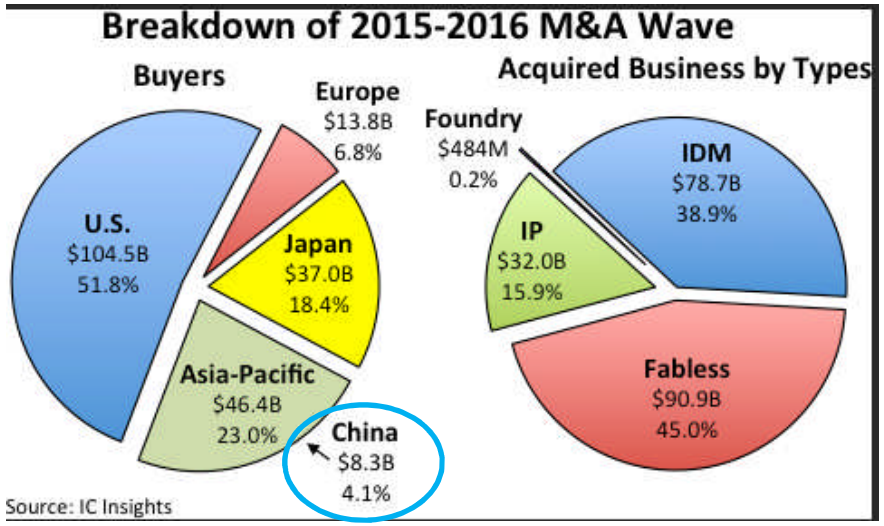
- **Japan**
  - Trade and industrial actions in ‘70s & ’80s to increase market share in semiconductor industry
  - Largely successful, U.S. lost significant market share and fab capacity.
  - SEMATECH formed, in part, to establish domestic capability in tools in light of these trends
- **Taiwan**
  - Created ITRI in ‘70s, a government funded R&D Institute
  - Spun off multiple companies, including TSMC
  - Today has 4th largest segment of global market share and TSMC is world’s largest Pure-Play Foundry.
- **China**
  - In 2015, announced plan to reach “advanced world-level in all major segments of the industry by 2030.”
  - Using the following tactics:
    - Subsidies
      - $150 Billion over next 10 years, roughly size of US commercial industry average spending
      - Direct funding of state owned organizations (chiefly TsingHua Unigroup).
      - Subsidizing purchases of foreign companies and IP
    - Zero-Sum trade policies
      - Influencing domestic customers to only buy from Indigenous Chinese semiconductor suppliers
      - Lack of respect for IP rights
      - Significant Mergers and Acquisitions activities
  - Current status:
    - Wafer foundries currently 2-3 generations behind in technology nodes (at 40nm in volume today, 28nm capability at SMIC planned by 2018)
    - No domestically owned memory producing commercial volume
    - Greatly increasing # of fabless firms, but no Tier 1 Equipment Firm

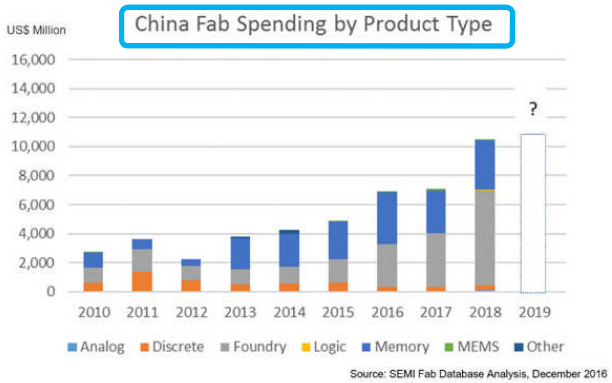
Technology Slow down due to sub-micron physical limitations provides an industry timeline gap to enable Chinese to rapidly advance.

https://goo.gl/nRWmPk

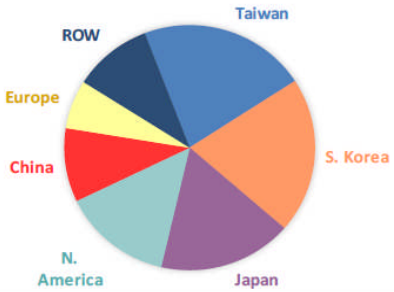
Industry Trends Likely to Continue

- **Trend towards fewer suppliers will likely continue**
  - Semiconductor Related Mergers and Acquisitions have accelerated in the past two years[1]
    - 2010-2014 Average $12.6B/year
    - 2014-2015 Average $100.9B/year
  - "China's goal of boosting its domestic semiconductor industry has added fuel to the M&A movement" [1]
- **China's share of worldwide capacity is anticipated to increase**
  - Growth to 15% of world wide capacity anticipated by 2021[2]





Wafer Capacity at Dec-2015 – by Geographic Region
(Monthly Installed Capacity in 200mm-equivalents)



Region	Installed Capacity (K w/m)	% of Worldwide Total
Taiwan	3,547	21.7%
S. Korea	3,357	20.5%
Japan	2,824	17.3%
N. America	2,320	14.2%
China	1,591	9.7%
Europe	1,046	6.4%
ROW	1,665	10.2%
TOTAL	16,350	100%

Source: IC Insights

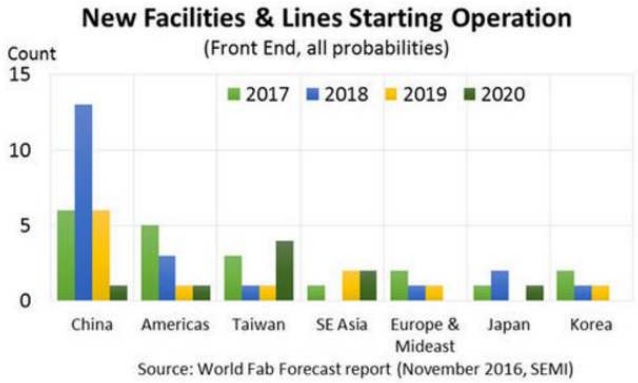
IC Insights: Global Wafer Capacity 2016-2020

(1) http://www.icinsights.com/news/bulletins/20152016-Deals-Dominate-Semiconductor-MA-Ranking/
(2) http://www.semi.org/en/fab-investment-surge-china-0

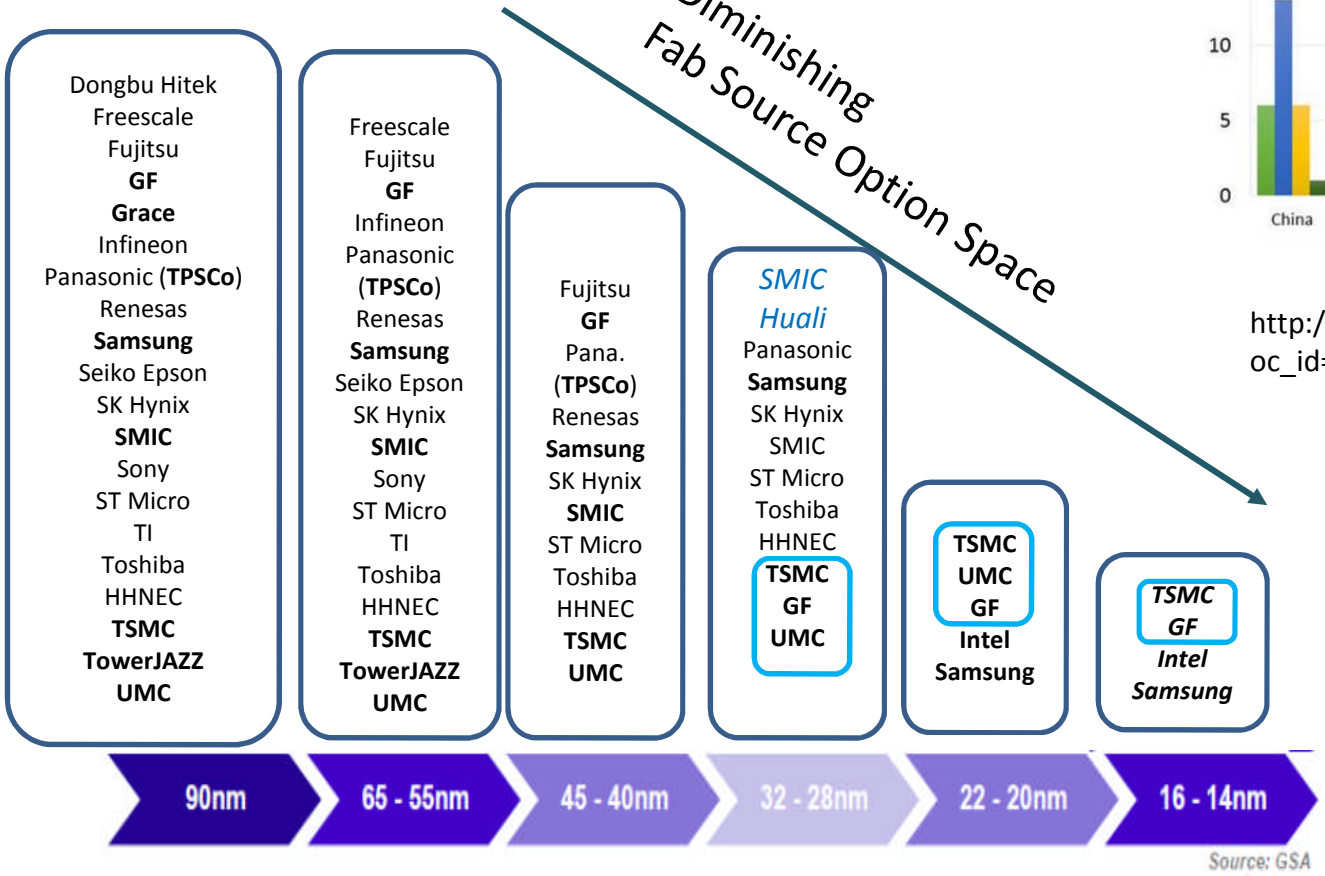
https://goo.gl/nRWmPk

Fab Source Option Space

NDIA



http://www.eetimes.com/document.asp?doc_id=1331002



Bold denotes foundry manufacturing providers

pure-play semiconductor foundries at leading edge (28nm and smaller)

Fabs being built

Derived from a chart originally from GSA

https://goo.gl/nRWmPk

Importance of IP at Advanced Nodes

- **Advanced nodes require advanced IP**
  - Technology features can not be leveraged without
  - Advanced IP typically carries longer lead times, higher cost than prior generations, and higher risk
- **Design migration / new designs in advanced nodes include increasingly complex IP / functionality to achieve greater capabilities (advantage)**
- **Leveraging commercially available IP is critical to DoD program schedules and cost control**
- **Re-creating advanced IP is not viable**
  - Costly, requires skilled critical resources, and adds significantly to project schedule and risk
- **Advanced node access MUST include access to leading edge commercial IP**
  - Funding
  - Countermeasures

https://goo.gl/nRWmPk

Acquisition Reform for Commercial

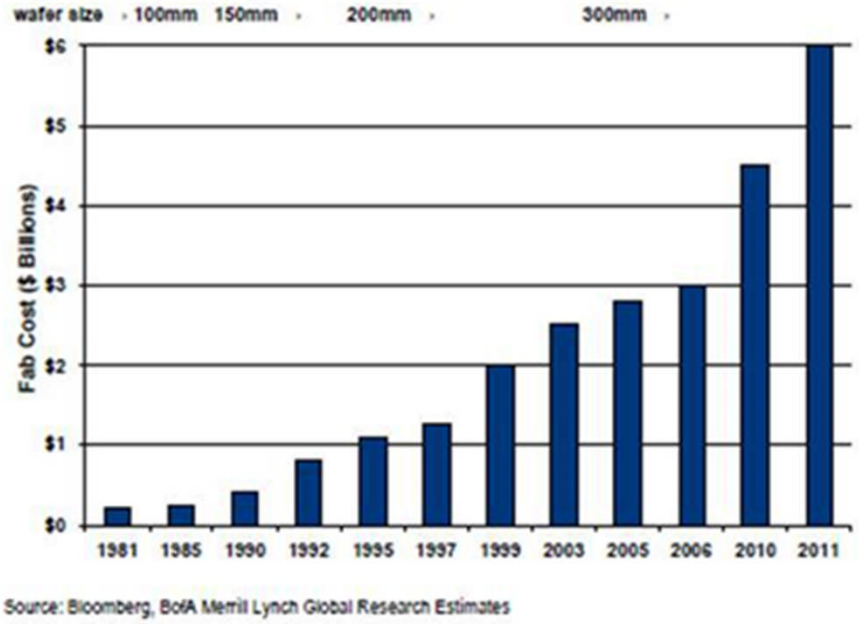
"If You Want Commercial, You Need to Act/Buy Commercial"

- Fund and execute commercially aligned pathfinder/prototyping projects to train DoD acquisition workforce
  - Leverage DARPA and ASD(R&E) projects
- Develop DoD microelectronics projects in a manner leveraging commercial best practices for technology selection, development cycles, and funding profiles
  - Adopt commercial company mindset when developing requirements, verification, product life cycle forecasting and procurement, and cost efficiency
- Contract Commercially
  - Leverage OTA and/or FAR Chapter 12 to greatest extent possible to better align with the commercial market, minimize flow downs
  - Strategically change acquisition regulations to make it easier for the government and Primes to contract from commercial suppliers

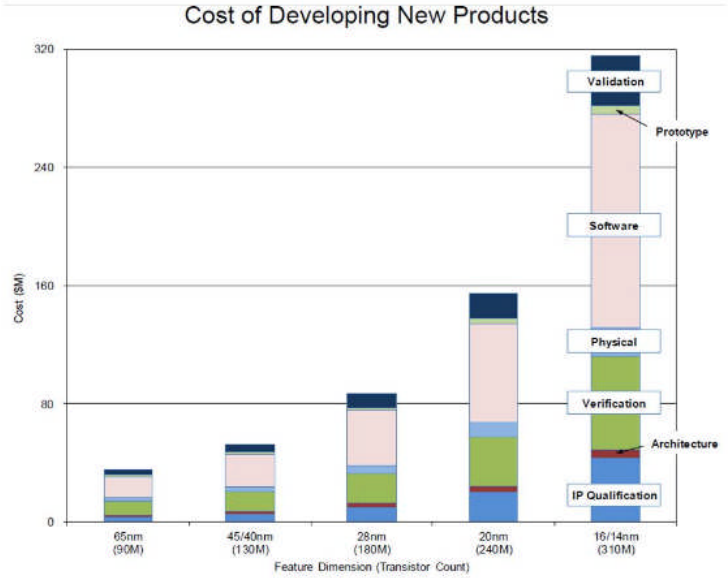
https://goo.gl/nRWmPk

Economies of Scale

- **Increasing fab costs at advanced nodes means that semiconductor fabrication is now economically possible only at high manufacturing volumes**
- **Increased design costs means that Customer business cases favor high product volume solutions vs. niche products**



Source: Bloomberg, BofA Merrill Lynch Global Research Estimates



Source: IBS

http://semiengineering.com/how-much-will-that-chip-cost/

https://goo.gl/nRWmPk

Aggregation of Production

- **Aggregate Production of Mil/Aero and ASIC parts, with commercial semiconductor suppliers, is needed to increase volume**
- **Key Issue**
  - Volume is needed by microelectronics industry for a valid business case
  - TAPO aggregates DoD program specific programs and is a model that works for DoD
  - An aggregated solution, to support industrial production for catalog items, is also needed
- **Path for use of TAPO office for industrial production?**
  - Aggregate additional volume
  - Adopt policy or other regulations, for other critical infrastructure applications, to leverage supplier base
- **Defense Production Consortium Concept?**
  - Structured like MOSIS/ISI except for production
    - Focused totally on low volume
    - Multi-Project Wafers? Multi Layer Masks?
  - National Cooperative Research and Production Act (NCRPA) of 1993
  - Open to anyone who wants to order
    - Maybe have membership fee for consortium
  - Defense support ($$?) for "access"
    - Access to production partners and defense specific technologies (like RH)
  - Issues
    - Anti-Trust, NCRPA says that with approval you are not liable to treble damages, but
    - Can't structure consortium to damage the business of foundries

https://goo.gl/nRWmPk

Aggregation of EDA S/W and IP

- **Key Issue – low volume reduces the ability to obtain EDA S/W and IP (Mil/Aero)**
  - Organizations that can't do design "at scale" incur exponential costs
- **Proposed concept of USG (or Service/Agency) wide licensing isn't a solution**
  - Although intramural R&D wants to get access to EDA/IP, that is not the problem
  - Mil/Aero Microelectronics Industry is being priced out of EDA/IP access
  - EDA/IP unlikely to license to entire M/A Microelectronics industry (dual use)
- **Two potential approaches: (1) Defense Design Consortium, and (2) Defense Design Centers of Excellence**
- **Defense Design Consortium**
  - Members join (for a fee)
  - Consortium licenses EDA/IP from commercial vendors
  - Maintains a Trusted IP library, accessible to all members
  - Members assign staff to the Consortium to do designs on Consortium capabilities
  - Maintains a Trusted IP library, accessible to all members
- **Defense Design Centers of Excellence**
  - Defense support for one or more industrial centers (supports EDA/IP from commercial vendors)
  - Industry subcontracts with center to design and/or jointly design new products
- **Would these business models work for commercial EDA and IP providers?**

https://goo.gl/nRWmPk

21st Century SoC Requirements

Are DoD System on Chip (SoC) requirements changing for advanced nodes?

- SOCs include Digital, RF, Mixed Signal, or mix-and-match applications
- DoD SoC requirements include unique requirements above commercial, such as
  - military temp. range, hermetically sealed packages, reliability, radiation tolerance
  - Unique security and trust requirements
- **No new or additional DoD requirements, above and beyond commercial, were identified specifically for advanced node applications**
- **However, it has become more difficult at advanced nodes to maintain the same requirements due to the following factors:**
  - Commercial Pace of Technology Development
  - Increase in node design complexity
  - Increase in integrated functionality and 3rd party IP content
  - Increase in thermal density
  - Distribution of end to end workflow elements to world wide suppliers

https://goo.gl/nRWmPk

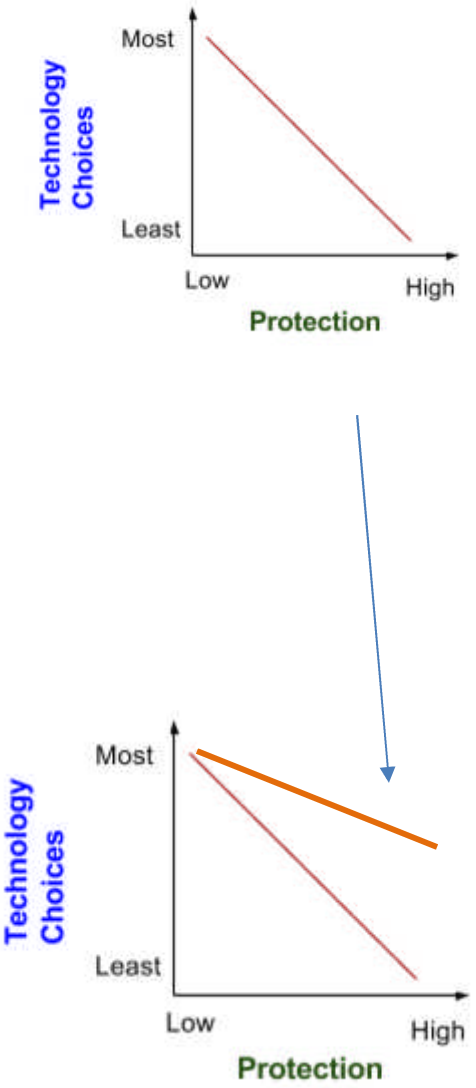
21st Century SoC - Ideas to Consider

- **Align with commercial specifications**
  - Mil temp and high reliability – align with Automotive specs?
- **Align with commercial "building blocks"**
  - Architecturally, leverage commercial investments, with overlay of assurance approaches
- **Align with commercial tools and standards**
  - Don't re-invent it for the DoD…
- **Move system architecture standards to SOC implementations**
  - Recognize these chips are systems on chips
- **Adopt security practices from commercial industry**
  - High security requirements for certain commercial applications – can they be adopted?
- **Promote a business model and culture for assured re-use across disparate programs and commonality for scale**

https://goo.gl/nRWmPk

Trust and Security

- **Trusted sourcing for mission critical integrated circuits is required per DoD policy 5200.44**
- **Trusted accredited suppliers, under the current Trust criteria, do not exist for nodes below 32nm**
- **Various Countermeasure techniques are being developed, by DARPA and others, to achieve security across end to end workflow elements**
- **A/CM analysis techniques could lead to a more nuanced approach for application of sufficient security at each step in the end to end flow**
  - Accounts for supplier workflow element risk analysis
  - Accounts for program level application of countermeasures
- **A new approach in how we achieve security could open up access while satisfying security – achieving availability of advanced technologies to DoD programs**

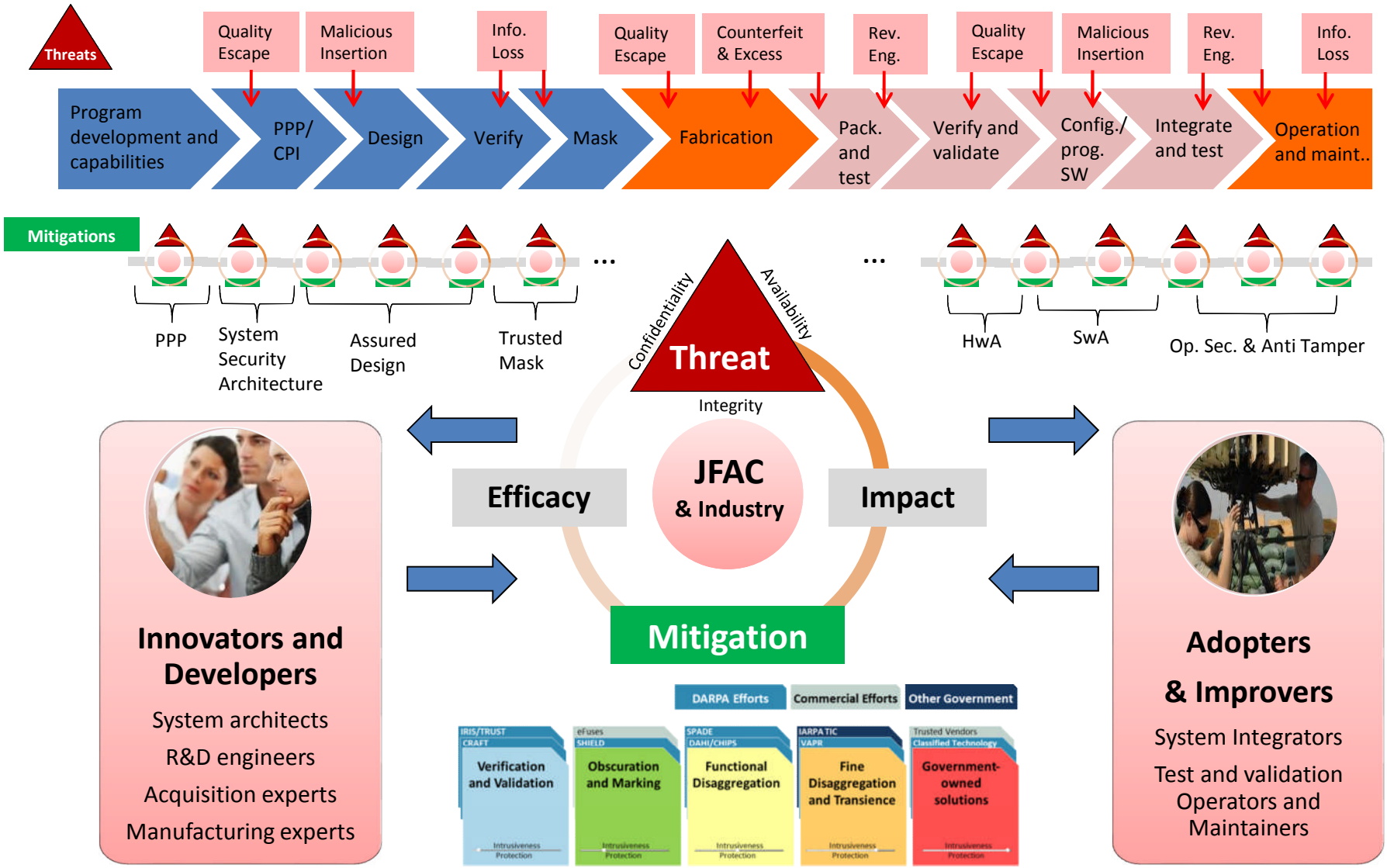


https://goo.gl/nRWmPk

(1) Consequences
(2) Impacts
(3) Actions

Systems Engineering Approach

NDIA



Dr. Jeremy Muldavin Office of Deputy Assistant Secretary of Defense, Systems Engineering (DASD(SE))

https://goo.gl/nRWmPk

New Trust Model Goals?

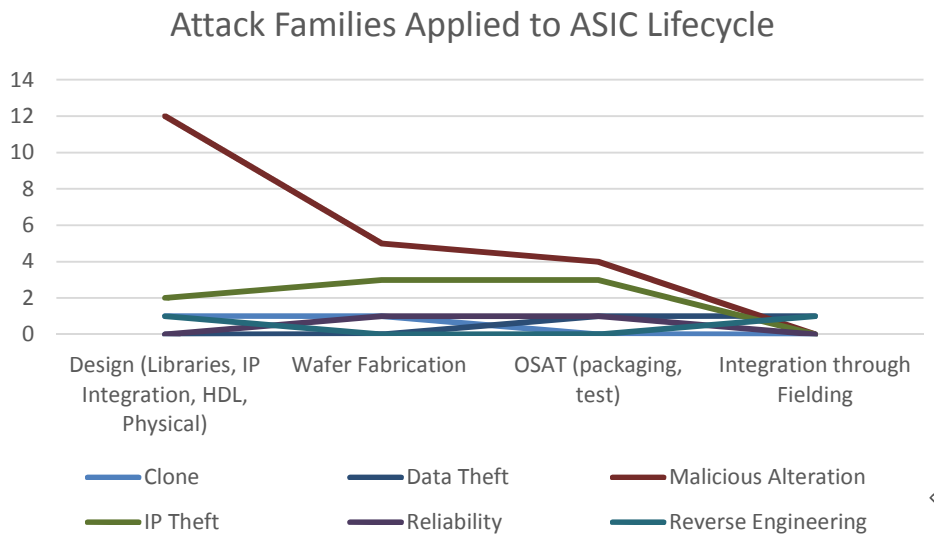
- **Today's options**
  - Use existing Trusted accredited suppliers for end to end workflow elements available
    - Not all end to end workflow elements are available Trusted
  - Obtain a waiver to 5200.44 via a program protection plan for a specific program
    - Discouraged / not supported today and requires extensive effort/time
- **Potential for a New Process to address the following elements:**
  - End to End workflow element Attack vulnerability assessment
  - End to End workflow element countermeasure assessment
  - Data base for results
  - Program level assessment means

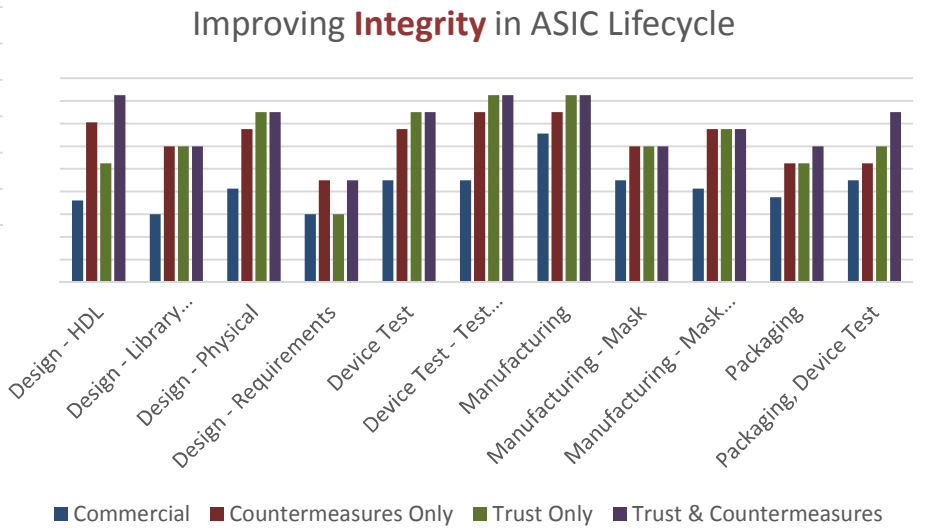
  → This could enable optimal selection of available and secure end to end flow elements for each program

https://goo.gl/nRWmPk

E2E Workflow Vulnerability Assessment

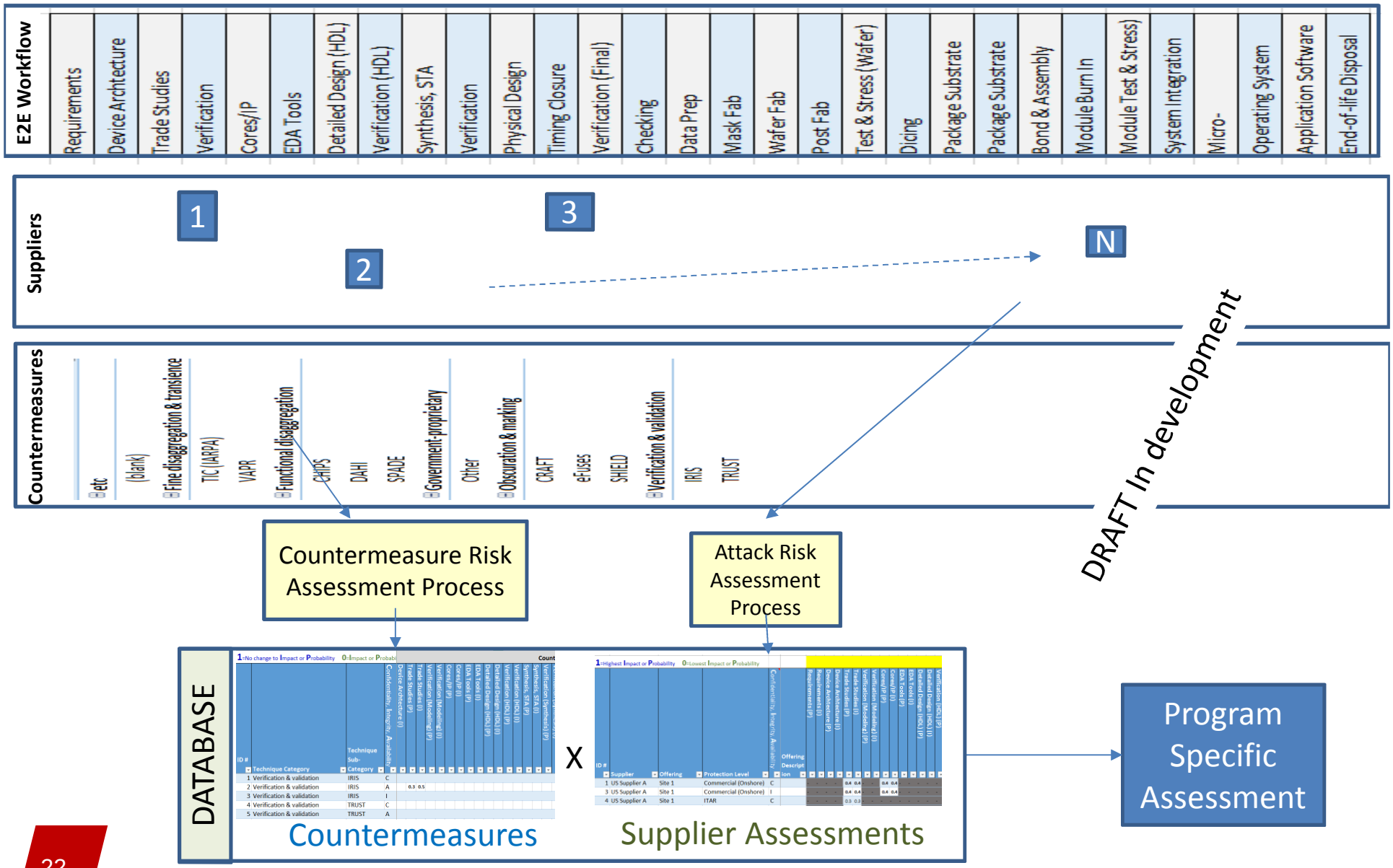
- **Evaluation of attacks that could be executed across the ASIC development lifecycle provides insight into areas of particular vulnerability.**
- **Application of countermeasures, trust, or both, can improve assurance of devices, and target assurances**





https://goo.gl/nRWmPk

Sketch of Trust Assessment Tool



https://goo.gl/nRWmPk

Need for a National Strategy

- **The U.S. currently has no national manufacturing strategy for semiconductors; ideally such a policy would encompass:**
  - Research
  - Strategic investment
  - Measures to mitigate the high costs of serving the defense market
  - IP protection
  - Tax Policies
  - Public-Private Partnerships
- **In contrast, China has adopted a five year plan and partnerships with Regions and localities with very specific goals:**
  - Manufacture 70% of country's demand by 2025
  - Investing $100–$150 Billion over next 10 years to buy, collaborate, and obtain capabilities
  - $ 70B investment for advanced Memory Fabs in 2017
- **Public-private partnerships have been successful in advancing public and private technology development goals and should be considered further**

https://goo.gl/nRWmPk

Public-Private Partnerships

- **Public-private Partnerships serve to:**
  - Provide commercial industry access to manufacturing infrastructure, toolsets and possibly IP for pre-A and A round investments
  - Provide USG access to technologies at the leading edge and those that are not otherwise commercially viable
  - Mitigate financial risk for commercial industry
  - Create jobs and provide economic stability
- **PPPs can be sustained by a diverse revenue stream, including:**
  - Public Grants
  - R&D contracts, public or private
  - Membership fees
  - IP licensing revenue
- **There are many past and present examples of successful public-private partnerships in semiconductor and other technology heavy industries.**
  - IMEC (Belgium), ITRI (Taiwan), A*Star (Singapore), Sematech (U.S.)
  - Manufacturing USA (NNMI) attempting this for manufacturing in general. Could be leveraged to benefit the semiconductor industry (https://www.manufacturing.gov/nnmi/)
  - Expanding beyond two current semi-focused manufacturing institutes is possible tool

Public-Private Partnership Recommendations

- **We endorse the trade, tax and intellectual property rights high-level recommendations made by the recent PCAST Working Group on Semiconductors.**
- **We also recommend:**
  - Establish Public-Private Partnerships to support manufacturing learning and intellectual property development:
    - Technology Acceleration Initiatives focused on specific challenges, such as materials development and integration
    - Shared Facilities for prototype development, testing & validation, low volume production for USG and accelerate development of anti-tamper measures
  - Create environment for broad demand for trustable microelectronics to increase demand and lower the cost
    - Critical industrial infrastructure applications such as autonomous vehicles, finance, air traffic control systems, and defense systems

https://goo.gl/nRWmPk

Q&A Session

We value your interaction today!

Please provide any additional feedback with the form: https://goo.gl/nRWmPk

Please Vote for areas that you request this group to focus on: https://goo.gl/5zOWsG