Automatic Test Committee – 2016 Status

2016 Tasks Planned	Status	Accomplishments (deliverables, etc.) - Comments
FPGA Test and Support	Ongoing	Status: •Mike Dewey assigned as leader. Group formed, met 11.18. Next meeting 12.15. •Agreed that a SOW will be created which defines the goal / output of this group. Overall timeline would be to have a SOW ready for review by NDIA ATS committee in the Q1/17 timeframe. Overall effort would be 8 months for completion of this task.
Standardized Software Architecture for Synthetic Instrumentation	Ongoing	Status: •Mike Seavey assigned as leader. •Need to define next steps.
Cyber Security	Deferred	Status: Will be discussed as part of FPGA effort. Cyber security is a big concern when using FPGAs that are programmable. Offers another entry path for malware / security breaches. How do you allow reprogramming without compromising cyber security? • Concern when connecting a UUT to the tester which has an FPGA, can infect the tester and then can propagate to other UUTs

Automatic Test Committee – 2017 Task Plan

Proposed 2017 Tasks:

- Government/Industry Liaison Reports
- ATC projects:
  - FPGA Test and Support
  - Standardized Software Architecture for Synthetic Instrumentation
  - Cyber security (deferred)

Deliverables / Products:

- Semi-annual Reports posted on ATC Web-site:
  - US Army ATS Liaison Report
  - USAF ATS Liaison Report
  - US Navy/USMC-Air ATS Liaison Report
  - USMC-Ground ATS Liaison Report
  - DoD AMB Liaison Report
  - Commercial ATS Liaison Report
- Develop SOW and first draft reports for the FPGA Test/Support and Software Architecture for Synthetic Instrument projects

Schedule / Resources

Status/Review/Present at regular ATC meetings:

- March/April at NDIA HQ
- September adjacent AUTOTESTCON in Chicago, IL
- December with SED (TBD)

Project Meetings held as required

Issues / Concerns:

Limited Budget/resources:

- ATC is focusing on high value projects, deferring lower priority projects.