NDIA
Automatic Test Committee
Project Report

September 10, 2017

Renaissance Schaumburg ATC17

Overview

- **Two projects identified by US Government ATS leadership for industry investigation**
  - FPGA Test and Support
  - Standardized Software Architecture for Synthetic Instrumentation

FPGA Test & Support Background

- **Issues include**:
  - Multiple manufacturers, each with their own sets of development tools.
  - Programming data not consistent between manufacturers for the same functionality.
  - Where to put the emphasis in FPGA test? TPS or ATE or somewhere in between? How do we control the interface boundaries between vendor, ATE, and TPS programming?
  - No DoD standards or programming style preferences. This can lead to portability problems and obsolescence issues.

FPGA Test & Support Project

- **Group Leader:** Mike Dewey
  - Group members from industry, US Navy, US Army and US Air Force
  - Meeting monthly via telecon
- **Objective:** Define Goals via SOW & Develop Recommendations and Guidelines
- **Status:**

  1) SOW created and approved by NDIA ATS committee

  2) Recommendations & Guidelines created & delivered
- **Next Step:** Receive feedback from NDIA ATS committee

FPGA Test & Support Project SOW

Statement of Work – NDIA ATC Project

Incorporating User Programmable FPGA Designs into ATS Applications – Recommendations and Guidelines

Prepared by: Mike Dewey, Carl Helde, Pat Griffin, additions from RWL & JRB
Revision: R4
Revision Date: 3/28/2017

Purpose

This statement of work defines the framework / outline for the creation of a document that will provide recommendations / guidelines when incorporating user programmable" or "user-defined" Field Programmable Gate Array (FPGA) devices / designs into an Automatic Test System (ATS). In addition, the document will provide guidelines / recommendations regarding the adoption / feasibility of user defined FPGAs for ATS applications. In this community the ATS includes the Automatic Test Equipment (ATE), Test Program Set (TPS), Interface Test Adapter (ITA) applications, and documentation.

The purpose of the resulting document is to provide developers of test systems and test programs that employ user-programmable FPGA devices and modules, guidelines regarding the use of user programmable FPGAs as well as facilitating maintainability and extended life cycle management of both systems and test programs. This statement of work details the targeted audience, what will be addressed, what will not be addressed, and an overall timeframe for completion of the final document.

1. Targeted Audience

- Suppliers of test systems / applications to the DoD services that incorporate user-programmable FGPA devices and modules that are incorporated into a test system's instrumentation, ITAs and associated test programs
- Test engineering managers and test engineers developing test programs that include user-programmable FPGA devices and modules as a component of a test program or test system
- Personnel associated with contracting and/or acquiring ATS equipment and applications that may incorporate user programmable FPGA devices and modules
- Standards organizations - e.g. IEEE, VXI P&P, etc., should the resulting document be managed and adopted by one of these standards organizations

2. What will be addressed in the document

1. Best practices for ensuring long term and organic support for test systems and applications that employ user-programmable FPGA devices and modules
2. Use of user-programmable FPGA device and module design tools that promote long term sustainability.
3. Use of Intellectual Property (IP) and associated data rights that will promote organic support and long term sustainability of test systems that employ user-programmable FPGA devices and modules.
4. Configuration management / documentation methods for user-defined FPGA applications
5. Use of user-programmable FPGA devices and modules in conjunction with test programs and associated ITAs
6. Identify and define the use of standardized interfaces that communicate and control IP that is part of an FPGA device or module in order to facilitate organic / long term support of test systems that employ FPGA-based designs as well as facilitating the use of FPGAs from various vendors
7. Define a standardized policy for sustaining designs / TPS that employ user-programmable FPGA devices and modules.

Statement of Work – NDIA ATC Project

Incorporating User Programmable FPGA Designs into ATS Applications – Recommendations and Guidelines

8. Identify / define the use of IEEE standards for configuring / programming of user-programmable FPGA devices and modules
9. Investigate the feasibility of transitioning this document to an open, industry standard which can be managed by an industry standards group.

3. What will not be addressed in the document

1. Cyber security management as it relates to user programmable FPGAs. It is acknowledged that the use of programmable devices including FPGAs represents a cyber security threat which can be susceptible to malware and viruses. However, addressing cyber security as part of this current effort is a topic best addressed as part of a future project that can encompass all potential cyber threat avenues – test programs, programmable devices, network connections, etc.
2. Instrumentation or test systems that employ FPGAs which are non-accessible by the end user. Virtually all instruments and test systems are now including programmable devices. However, the task for this project needs to be focused on addressing those applications that employ "user programmable" FPGA devices. FPGA devices that cannot be accessed / programmed by the end user are not part of this effort.

4. Proposed timeline for this project

The estimated timeline for this project is as follows:

- Initial SOW creation and review by the project working group: End of January 2017
- Updates to SOW and submission to NDIA ATC for review and agreement: End of February 2017
- Development of document: March – June 2017
- Review and updates: July 2017
- Final review and release of document by NDIA ATC: August 2017

End of SOW

FPGA Test & Support Project

Recommendations & Guidelines

Table of Contents 3

FPGA Test & Support Project

Recommendations & Guidelines

Appendix A maps the SOW's Section 2 items to the applicable sections in this document. The purpose of this section is to ensure that this document addresses the key areas Identified as requirements in the SOW.

SOW Requirement	Referenced Section in FPGA Recommendations Document
Best practices for ensuring long term and organic support for test systems and applications that employ user-programmable FPGA devices and modules	Section 5
Use of user-programmable FPGA device and module design tools that promote long term sustainability.	Section 5
Use of Intellectual Property (IP) and associated data rights that will promote organic support and long term sustainability of test systems that employ user-programmable FPGA devices and modules.	Section 9
Configuration management / documentation methods for user-defined FPGA applications	Section 8
Use of user-programmable FPGA devices and modules in conjunction with test programs and associated ITAs	Sections 2, 3 & 4
Identify and define the use of standardized interfaces that communicate and control IP that is part of an FPGA device or module in order to facilitate organic / long term support of test systems that employ FPGA-based designs as well as facilitating the use of FPGAs from various vendors	Section 6
Define a standardized policy for sustaining designs / TPS that employ user-programmable FPGA devices and modules	Not addressed. Definition of a policy or standard goes beyond the scope of this document which is to provide recommendations and guidelines. We would suggest that based on this document, the NDIA ATS group can decide if a policy / standard should be established that addresses the incorporation of user FPGAs as part of a TPS or ATE system.

Standardized Software Architecture for Synthetic Instrumentation

- This is not a new project but has come back to the committee as something we should explore.
- Originally was examined in 2014. Wade Lowdermilk and Dave Carey presented Trade Study.
- ATS chair asked DoD attendees to discuss the need for this project at the next AMB and NxTest IPT meetings. Howard will report on this activity.
- Lead for project – Mike Seavey
- **Will need to establish a team if Howard reports specific requests from AMB and NxTest IPT.**