**Trusted Microelectronics Special Topic:  
Field Programmable Gate Array (FPGA) Assurance**

February 27-28, 2018

Agenda

**February 27, 2018**

8:00am – 8:15am Welcome to MITRE (Bob Martin or Roberto Landau)

8:15am – 8:30am Welcome by NDIA Electronics Division Chair, Kelly Hennig, NGC

8:30am – 9:00am Welcome – Robert Gold, Director Enterprise Engineering, DASD(SE)

9:00am – 9:15am Workshop Charter and Organization – Gabe Mounce, USAF/AFRL

9:15am – 9:30am Highlights of the NDIA FPGA Assurance Workshop of March 1-2, 2017 – Brian Cohen, IDA

9:30am – 9:45am JFAC FPGA Assurance Risk and Mitigation Subgroup – Mike Johnson, SNL

9:45am – 10:15am JFAC FPGA Assurance Collaboration Subgroup - Gabe Mounce, AFRL

10:15am – 10:30am break

10:30am – 12:00pm JFAC FPGA Assurance Strategy, Policy and Guidance Subgroup

DOD FPGA Assurance Strategy – Ray Shanahan, DASD(SE)

Discussion

12:00pm – 1:00pm Lunch on your own (MITRE Cafeteria available)

1:00pm – 1:45pm Review of Trusted and Assured Microelectronics Program FPGA Assurance Activities – Jeremy Muldavin, DASD(SE)

Discussion

1:45pm – 2:00pm Recent Title III and SBIR Activities – Gabe Mounce, USAF/AFRL

2:00pm – 2:30pm ASIC/FPGA Trust Assessment (AFTA) Framework– Melanie Berg, NASA and Vik Rao, Aerospace

2:30pm – 2:45pm Break

2:45pm – 3:45pm FPGA Vendor Panel, Mike Johnson

Steve McNeil, Xilinx

Ryan Kenny, Intel PSG

Paul Quintana, MicroSemi

3:45pm – 4:45pm eFPGA Ecosystem Panel, Matt Casto, AFRL

Andy Jaros, Flex-Logic

Roger Brees or Warren Snapp, Boeing (invited)

Steve Svoboda, Menta (invited)

Mentor? (Pending)

4:45pm – 5:00pm Discussion and Wrap-up for the Day

**February 28, 2018**

8:00am – 8:15am Welcome to MITRE (Bob Martin or Roberto Landau)

8:15am – 8:45am Risk Assessment in FPGAs for Mission Assurance – Michael Vai, MIT-LL

8:45am – 9:45am Engineering with FPGAs – A User Perspective Panel – Melanie Berg, NASA

Marco Figueiredo (Orbital)

Dominic Lucido (Mentor Graphics) (invited)

Danny Chan (Raytheon) (invited)

9:45am – 10:00am Break

10:00am – 11:00am FPGA Design Assurance Panel – Brian Cohen

Joe Jarzombek, Synopsys

John Hallman, MacB

Jason Oberg, Tortuga

11:00am – 12:00pm Wrap-up Discussion

Feedback on Strategy

Gaps???

12:00pm – 1:00pm Lunch on your own (MITRE Cafeteria available)

**Convene Classified Session – Room is cleared**

1:00pm – 2:00pm Trust in FPGA Deep Dive – Mike Johnson, Sandia

2:00pm – 3:00pm FPGA Assurance Strategy (secret) – Ray Shanahan, DASD(SE)

Discussion

3:00pm – 4:00pm Discussion of Strategy – Ray Shanahan

4:00pm – 4:30pm Discussion Next Steps

4:30pm – 5:00pm Summary and Wrap-up for the Day