


# **NDIA**

## **TRUSTED MICROELECTRONICS SPECIAL TOPIC: FIELD PROGRAMMABLE GATE ARRAY (FPGA) ASSURANCE**



### **Agenda - Open Session**

**March 1-2, 2017**

**The MITRE Corporation, McLean, VA**



## March 1, 2017

- 11:45am – 12:45pm REGISTRATION
- 12:45pm – 1:00pm WELCOME TO MITRE  
Mr. Bob Martin, *Senior Principal Engineer, The MITRE Corporation;*  
or Mr. Roberto Landrau, *Principal Electronics Engineer, The MITRE Corporation*
- 1:00pm – 1:15pm WELCOME  
Mr. Robert Gold, *Director, Enterprise Engineering, ODASD(SE)*
- 1:15pm – 1:30pm OVERVIEW OF JFAC AND DOD ASSURANCE EFFORTS  
Mr. Ray Shanahan, *Deputy Director, Anti-Tamper Hardware Assurance, ODASD(SE)/EE*
- 1:30pm – 1:45pm WORKSHOP CHARTER AND ORGANIZATION  
Mr. Gabe Mounce, *Technology Commercialization Lead, AFRL, FPGA Collaboration Team Lead*
- 1:45pm – 2:45pm GOVERNMENT FPGA ASSURANCE PANEL  
Chair: Dr. Jeremy Muldavin, *Deputy Director, Defense Software & Microelectronics Assurance Activities, ODASD(SE)/EE*
- Mr. Aman Gahoonia, *Microelectronics Engineer, DMEA*
  - Mr. Mike Johnson, *Senior Engineer, Sandia National Labs*
  - Mr. Jeff Krieg, *Chief, Hardware Reverse Engineering Division, NSA Information Assurance Directorate*
  - Mr. Gabe Mounce, *Technology Commercialization Lead, AFRL*
- 2:45pm – 3:00pm NETWORKING BREAK
- 3:00pm – 4:00pm FPGA VENDOR PANEL  
Chair: Mr. Brett Hamilton, *Chief Engineer Trusted Microelectronics, JFAC Hardware Assurance Lead, NSWC Crane*
- Mr. Ryan Kenny, *Strategic and Technical Marketing, CISSP, Intel Corporation*
  - Mr. Steve McNeil, *Principal Engineer, Xilinx, Inc.*
  - Mr. Paul Quintana, *Director Vertical Marketing for Defense & Security, Microsemi Corporate*
- 4:00pm – 5:00pm FPGA SECURITY RESEARCH PANEL  
Chair: Dr. Matt Casto, *Senior Electronics Engineer, AFRL*
- Dr. Domenic Forte, *Assistant Professor, University of Florida*
  - Mr. Matt French, *Research Director, Information Sciences Institute*
  - Mr. Jonathan Graf, *Founder and CEO, Graf Research*



## March 2, 2017

8:30am – 9:00am	DESCRIPTION OF FPGA BREAKOUT GROUPS, MISSION AND GROUP ASSIGNMENTS
9:00am – 12:00pm	BREAKOUT SESSIONS
12:00pm – 1:00pm	LUNCH <i>(groups may elect to bring lunch back to their breakout rooms and work through lunch)</i>
1:00pm – 3:00pm	WRAP-UP GROUPS AND DRAFT BREAKOUT GROUP REPORT
3:00pm – 5:00pm	REPORT OUT FROM BREAKOUT GROUPS <i>25 minutes each</i>
5:00pm – 5:30pm	WRAP-UP AND NEXT STEPS