NDIA

TRUSTED MICROELECTRONICS SPECIAL TOPIC: FIELD PROGRAMMABLE GATE ARRAY (FPGA) ASSURANCE

Agenda – Government and FFRDC Only Session

March 1-2, 2017
The MITRE Corporation, McLean, VA

March 1, 2017

7:00am – 8:00am	REGISTRATION
8:00am – 8:15am	WELCOME Mr. Bob Martin, *Senior Principal Engineer, The MITRE Corporation; or* Mr. Roberto Landrau, *Principal Electronics Engineer, The MITRE Corporation*
8:15am – 8:30am	WELCOME Mr. Robert Gold, *Director, Enterprise Engineering, ODASD(SE)*
8:30am – 8:45am	UPDATE ON JFAC AND DOD ASSURANCE EFFORTS Mr. Ray Shanahan, *Deputy Director, Anti-Tamper Hardware Assurance, ODASD(SE)/EE*
8:45am – 9:00am	WORKSHOP CHARTER AND ORGANIZATION Mr. Gabe Mounce, *Technology Commercialization Lead, AFRL, FPGA Collaboration Team Lead*
9:00am – 9:45am	UPDATES ON FPGA ASSURANCE WORK SINCE LAST WORKSHOP • FPGA Trust Study – *Mr. Mike Johnson, Senior Engineer, Sandia National Labs* • Title III Trusted FPGA Project – *Mr. Gabe Mounce, Technology Commercialization Lead, AFRL* • Trusted FPGA – *Mr. Aman Gahoonia, Microelectronics Engineer, DMEA*
9:45am – 10:00am	NETWORKING BREAK
10:00am – 10:15am	REVIEW OF RESULTS FROM MAY 17, 2016 WORKSHOP Mr. Ray Shanahan, *Deputy Director, Anti-Tamper Hardware Assurance, ODASD(SE)/EE*
10:15am – 10:30am	FPGA ASSURANCE COLLABORATION SUB-TEAM Mr. Gabe Mounce, *Technology Commercialization Lead, AFRL*
10:30am – 10:45am	FPGA ASSURANCE RISK AND ASSURANCE SUB-TEAM Mr. Mike Johnson, *Senior Engineer, Sandia National Labs*
10:45am – 11:00am	FPGA ASSURANCE STRATEGY SUB-TEAM AND DISCUSSION Mr. Ray Shanahan, *Deputy Director, Anti-Tamper Hardware Assurance, ODASD(SE)/EE*
11:00am – 11:30am	REVIEW OF WORKSHOP PLAN AND BREAKOUT GROUPS
11:30am – 12:00pm	DISCUSSION OF WORKSHOP PLAN AND NEXT STEPS