

# DoD Trusted and Assured Microelectronics Summary

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## **Future Warfighting Needs**



### Dependency on Advanced Microelectronics Technology

#### Cyber & Quantum

 >1000x performance enhancement and efficiency for real-time ID/processing/response/security

#### Mesh Networked C3

- Open and distributed architecture to enable local processing of raw data on the battlefield
- Adaptive processing for multi-antennas and frequencies for robust comm. and radar systems

#### Artificial Intelligence and Autonomy

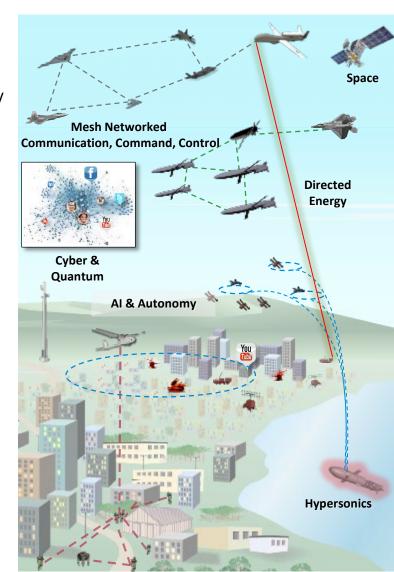
 Need vision, semantic, and navigation processing for high-performance imagers and navigation

#### Directed Energy

 Advanced Imagers, optoelectronic technology, signal processing and control systems, spectral awareness

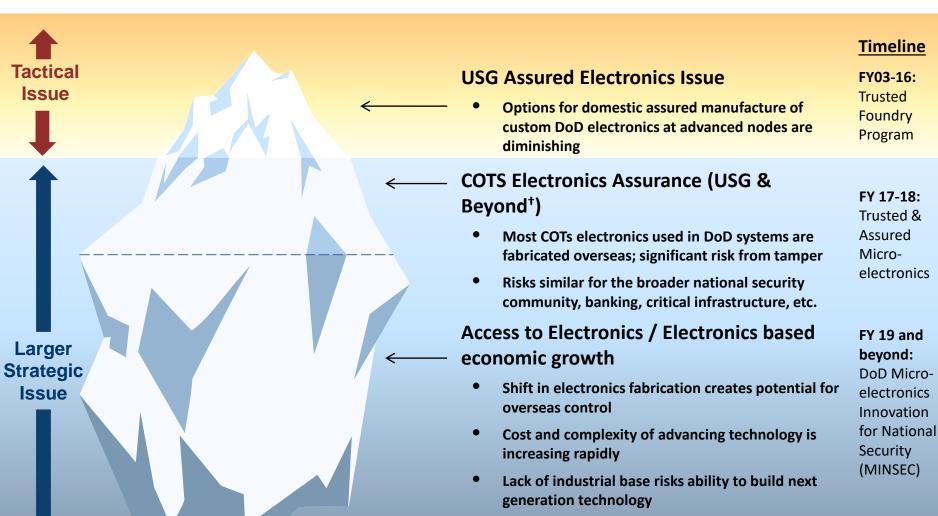
#### Space & Hypersonics

 Significant increases in rad-hard on-board sensor processing, communications, targeting, controls



## Strategic Microelectronics Issue





Significant Chinese investments represent a strategic national issue

<sup>†</sup> Including the broader national security community, banking, critical infrastructure, commercial industry, etc.

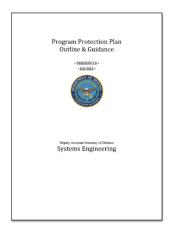
## Key Elements of DoD's Implementation Plan



- Revised microelectronics assurance policy and guidance to address state-of-the-art (SOTA)
  technology applications, use of commercial parts in DoD systems, and full life cycle vulnerability
  protection, beginning with secure design and protection of intellectual property (IP)
- Robust microelectronics verification and validation (V&V) capability
- Access to DoD/Government-unique needs, radiation-hardened by process and radiation-hardened by design technologies, in support of space and nuclear modernization, including Diminishing Manufacturing Sources and Material Shortages (DMSMS) foundry-of-last-resort capability
- Cultivation of workforce expertise and proactive engagement with academia, Defense Industrial Base (DIB), and DoD user communities in prototyping, and development activities to build a domestic knowledge base for design and manufacturing of advanced microelectronics
- Disruptive Research and Development (R&D) investment to lead development of the next generation microelectronics and protect domestic leadership
- Modernization of Defense Systems through advanced microelectronics technology and systemson-chips (SOCs), improving performance while reducing reliance on legacy parts and obsolete systems. Acquisition policies that promote rapid modernization, standards and best practices to facilitate V&V, supply chain risk assessment, and counterfeit detection
- Availability, Access and Assurance at multiple domestic SOTA Foundries through business models that sustain growth and commercial competitiveness

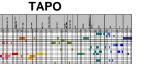
## **DoD Strategy and Actions**

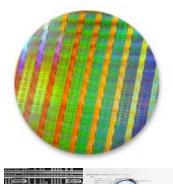




#### **Trusted Supplier Accreditation**

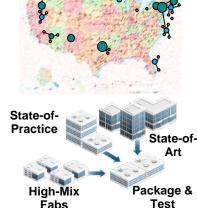












#### **Policy**

- Program Protection Plan (PPP), 5200.44, ITAR, DPA Title III updates
- Strategy/Directive for Assured Microelectronics
- National Security Strategy priority



#### **DMEA**

- Maintain and expand the number of trusted suppliers
- Provide access to state-of-the-art trusted flow (TAPO)
- Support sensitive needs and operations

### Trusted & Assured Microelectronics

- Assured Access to state-of-the-art foundries through modern trust and assurance methods and demonstration
- Industrial standards for assurance
- Joint Federated Assurance Center enhancements

#### **DoD MINSEC**

- Next generation R&D DARPA (ERI) captured in US
- Modernization & assurance for DoD & nation through Innovation ecosystems
- Radiation hardened micro-electronics for nuclear and space

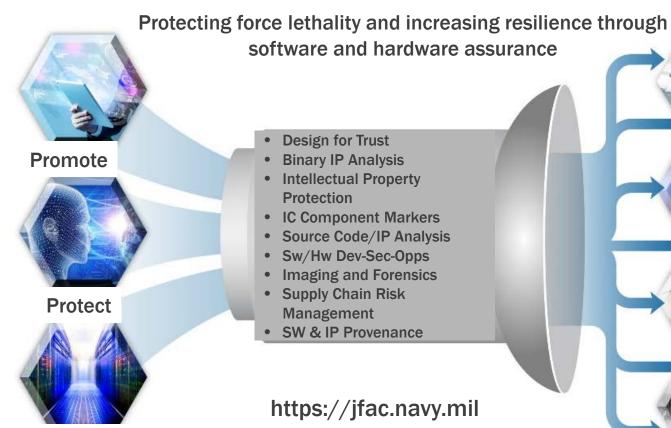
### Domestic Foundry & Packaging

- Multiple competitive State of the Art Foundries on shore
- Leadership in R&D and production
- Strong commercial business models
- Government business model for innovation & assurance

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## Joint Federated Assurance Center (JFAC)





**Design for Trust** 

- **Binary IP Analysis**
- Intellectual Property **Protection**
- IC Component Markers
- Source Code/IP Analysis
- Sw/Hw Dev-Sec-Opps
- **Imaging and Forensics**
- Supply Chain Risk Management
- **SW & IP Provenance**





**Partner** 

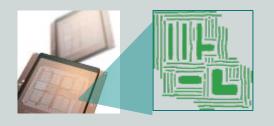
Federated Stakeholders - Army, Navy, Air Force, National Security Agency (NSA), Defense Microelectronics Activity (DMEA), Office of the Under Secretary (OUSD) of Defense (Research & Engineering), DoD Chief Information Officer, Defense Information Systems Agency (DISA), National Reconnaissance Office (NRO), Missile Defense Agency (MDA), OUSD (Acquisition & Sustainment), Department of Energy (DOE/NNSA)

## **T&AM Baseline Projects FY19**



#### Trusted Mask Trust Approach

- Secure trusted photomasks required for leading-edge designs
- Engage and support DoD programs to determine trusted photo-mask needs
- Leverages DPA Title III



## Verification & Validation (V&V) Capabilities and Standards for Trust

- Improve throughput and capability to analyze commercial parts using tools/techniques for leadingedge processes
- Provide destructive and nondestructive equipment, analysis tools, imaging software and highly skilled tradecraft
- Engage vendors to improve their device and IP security; acquire government access to specific proprietary designs, software, development and quality assurance processes and test procedures







## New Trust Approach Development and Demonstration

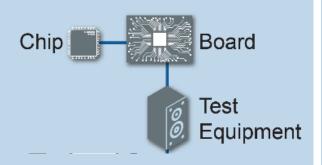
- S&T program of work to advance technologies and implement an alternative to the trusted foundry model
- Technologies include:
  - design for trust techniques;
  - IP partitioning and concealment;
  - split manufacturing;
  - cost-effective low-volume manufacturing;
  - tagging technologies to track chain of custody;
  - advanced imaging and forensics to evaluate dense components



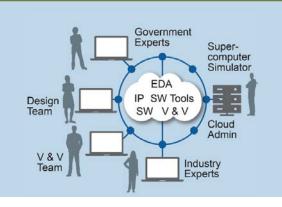
### T&AM Baseline Focus Areas



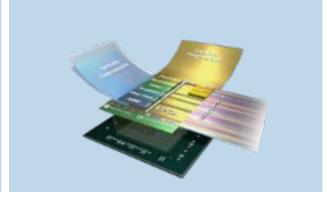
## Verification & Validation



## Design Assurance



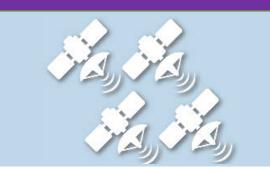
#### **FPGA Assurance**



## **Enhanced Manufacturing**



## Rad-Hard Microelectronics



## Outreach & Standards



## Microelectronics Innovation for National Security and Economic Competitiveness (MINSEC)





**Data Analytics** 

#### **Strategic National Security Applications**









Autonomous Systems + Al



Robust + Agile Communicators



**Commercial Space** 



**Biomedical** 

#### **Strategic National Economic Competitiveness Applications**

#### **Proactive** Awareness & Security

- Supply Chain track
- Proactive **Authorities**
- Intelligence & CI
- Standards

#### Access & **Assurance**

- Secure Design
- IP, EDA, experts
- · Foundry assured Access
- Modernization & co-development

#### **Enhanced** Manufacturing

- SOTP Back-end parity with SOTA
- SOTA on 200mm tools at SOTP
- High-mix low vol. fabrication

#### Incentives & **Market Growth**

- Acquisition reform and incentives
- · Tax, policy, regulation reform
- R&D and domestic fab incentives

#### Strategic **Alliances**

- Cooperative R&D
- Trade and Foreign Military Sales (FMS)
- Americas
- Europe
- Asia partners

#### **Disruptive Research & Development**

Experts, Infrastructure, Innovation, Venture Capital, Industrial Base, Academia

### **FY19 T&AM MINSEC Activities**



Enhancements	Description
Capture and Secure Microelectronics R&D	Supports secure design and capture of IP and architectures; IP sharing and re-use; and keeps DARPA ERI IP secure within the domestic ecosystem using secure design environments and domestic foundry capabilities.
New Microelectronics Development, Demonstration, and Capability Insertion	Supports public/private development of system-on-chip (SoC), hardware assurance, emulation and virtual verification and validation (V&V) to enable assured and secure IP; fabrication and packaging at SOTP government and merchant foundries; and design, packaging, testing, and integration of SoCs into a capability.
COTS programmable IC co-development	Pilots secure co-design capabilities and supply chain tools using commercially-available cloud-based services with/at commercial co-development partners to secure commercial IP and develop and promote security features and software and hardware assurance tools, and capabilities that meet future DoD needs.
Radiation-Hardened by Process (RHBP)/ Radiation-Hardened by Design (RHBD)	Provides for secure design and development of strategic radiation-hardened (SRH) IP and microelectronics test articles for JFAC and National Nuclear Safety Administration (NNSA) evaluation and qualification using RHBP techniques and SOTP foundry access.
Radio Frequency (RF) and Optoelectronic (OE)	Provides for secure design and development of radio frequency and optoelectronic IP and test articles, to include strategic designs, for JFAC and NNSA evaluation and qualification using SOTP and SOTA foundry access.
Microelectronics Obsolescence and Replacement	Supports critical process IP installation at two USG and/or a merchant foundry for USG use. This IP is required to ensure the continued availability of these critical technologies by providing for second sources.
Microelectronics-focused Workforce Development	Provide access to university, DoD, and small businesses for training and skill development; SOTA processes for test articles and training; and limited funding to promote design challenges and hacks around hardware IP development and assurance.

## DoD MINSEC Highlights (POM 19)



### Security య R&D

#### Develop the Next Generation Technology

DARPA Electronic Resurgence Initiative R&D Programs with matching from industry

Capture & Secure R&D in US Ecosystem Secure design environments, foundry access and enhancement, security support

Modernization & Security

**New Capability Development w/ Assurance &** Insertion into DoD, dual use products (1000x COTS)

**Assured COTS Programmable Co-Development** 

**Obsolescence & Replacement** 

**Workforce Development** 

**Rad-Hard Microelectronics** 

**RF & Optical Technologies** 

Deliver unique RF and optical technologies for DoD systems

#### **Results & Deliverables**









**Architectures** 







Secure design environments



Intelligence & counter intelligence



**Domestic** enhanced R&D fabs







Secure PNT SoC **EW** resistant



Assured FPGA from 2 vendors



2 Chips = 8 Peta FLOPS 400,000 FPS, 240W

10k X GPU

Preserve access to legacy IP and processes Future obsolescence replacement of boards by SoCs

100 STEM scholarships including microelectronics specialization

Specialty Needs

Deliver future nuclear and space modernization



- Domestic USG fab enhanced from 90nm AL to 65nm copper back-end process developed in partnership with NNSA
- Rad-hard by design developed for 1-2 SOTA foundry offerings with limited testing and qualification (strat-RH)



- Secure design and development of radio frequency and optoelectronic IP and test articles
- JFAC and NSA evaluation and qualification using SOTP and SOTA foundries

## DoD MINSEC Highlights (FY 19 Omnibus)



### Security య R&D

#### Develop the Next Generation Technology **DARPA Electronic Resurgence Initiative R&D** Programs with matching from industry

Capture & Secure R&D in US Ecosystem Secure design environments, foundry access and enhancement, security support

Modernization & Security

**New Capability Development w/ Assurance &** Insertion into DoD, dual use products (1000x COTS)

**Assured COTS Programmable Co-Development** 

**Obsolescence & Replacement** 

**Workforce Development** 

Specialty Needs

**Rad-Hard Microelectronics** Deliver future nuclear and space modernization

**RF & Optical Technologies** 

Deliver unique RF and optical technologies for DoD systems

#### **Results & Deliverables**









**Architectures** 





+Secure ments

design environ-

+Pilot **Innovation** Hub with Industry

+SOTA **Foundry** Access



+ATC Tech Pipeline for

+Pilot Secure SoC

+Pilot Reference **ASIC** Dev



+3D Packaging



**Assured SOTA & AI** 

+Promote security features and Secure Design **Assurance for COTs** 

- Preserve access to legacy IP and processes
- + Future obsolescence replacement of boards by SoCs
- +SOTA Access, Test articles, Training, Design Challenges, scholarships



- + Rad-hard reliability Eval (strat-RH)
- + Strat-RH test facility



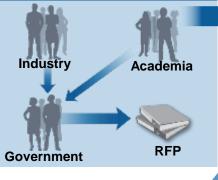
- JFAC and NSA evaluation and qualification using SOTP and **SOTA foundries**
- + Enhance SOTP Process Capabilities for DoD and Commercial

## New Capability Development Operational View

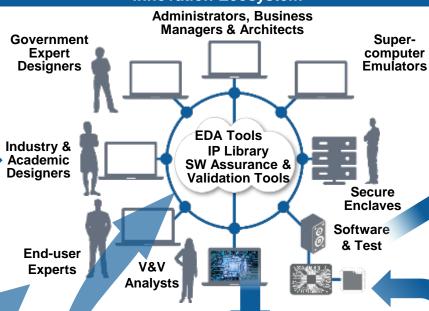




#### Innovators & Developers



#### **Innovation Ecosystem**





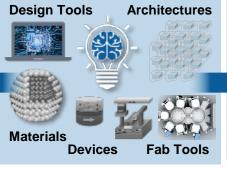
#### **Integrate & Demonstrate**



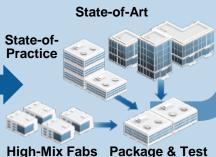
#### **Domestic Ecosystem**



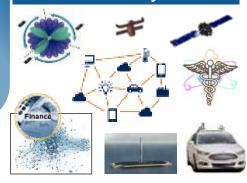
#### Research & Development



#### Fabricate & Package

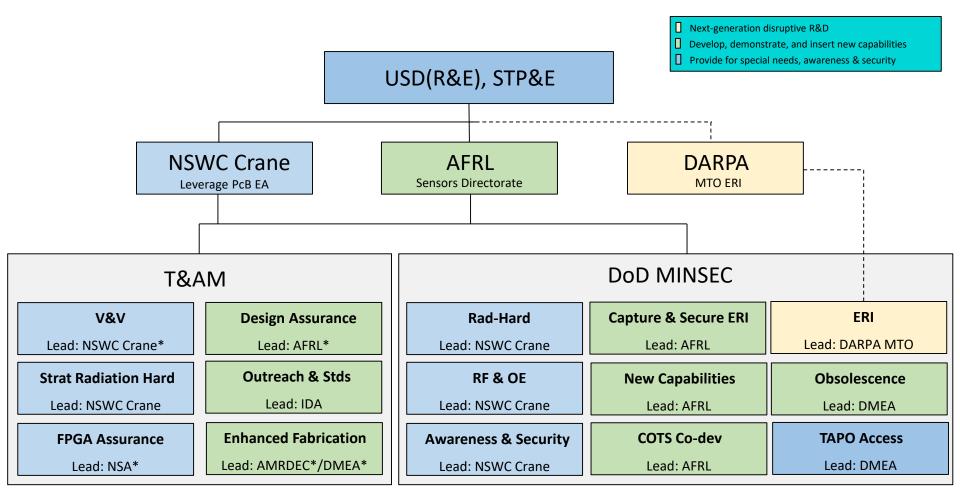


#### **Modernized Systems**



## T&AM & DoD MINSEC Execution Management





<sup>\*</sup>JFAC Federated Organizations, which include the Army, Navy, Air Force, National Security Agency (NSA), Defense MicroElectronics Activity (DMEA), Defense Information Systems Agency (DISA), National Reconnaissance Office (NRO), and Missile Defense Agency (MDA) laboratories and engineering support organizations; Intelligence Community and Department of Energy

## Summary



- Maintaining Technology Dominance is critical to economic and national security:
  - Promote and protect our critical missions, programs, and technologies
  - Combat adversary effectiveness and abilities to challenge our dominance
- Goals for Microelectronics Dominance and Semiconductor Leadership:
  - Revised trust and assurance standards that result in a competitive advantage for US/partners to deliver secure and reliable microelectronics
  - Maintain U.S. leadership in innovation and technology enabled by strong public/private partnerships to deliver next generation technology and capabilities
  - Maintain competitive domestic advanced microelectronics ecosystem and modern infrastructure (5G, smart cities, Al/autonomy, finance, IoT, etc.)

The DoD has been given an opportunity to take action towards these Goals in alignment with the whole government