



SRA Study Summary Report to NDIA Automatic Test Committee

June 15, 2010

Brian Miller

brian.miller@teradyne.com

978-460-1117

PIDESO

TERADYNE

Overall SRA Study Objectives

- Evaluate the trade-offs of current SRA test and diagnostic approaches (Government and Commercial) via initial analysis of NAVAIR repair requirements
- Identify opportunities for improving these current approaches
- Evaluate the feasibility of tailoring commercial techniques for the depot repair environment.

Process Overview

Select sample SRAs based on Cost, WIP, etc.

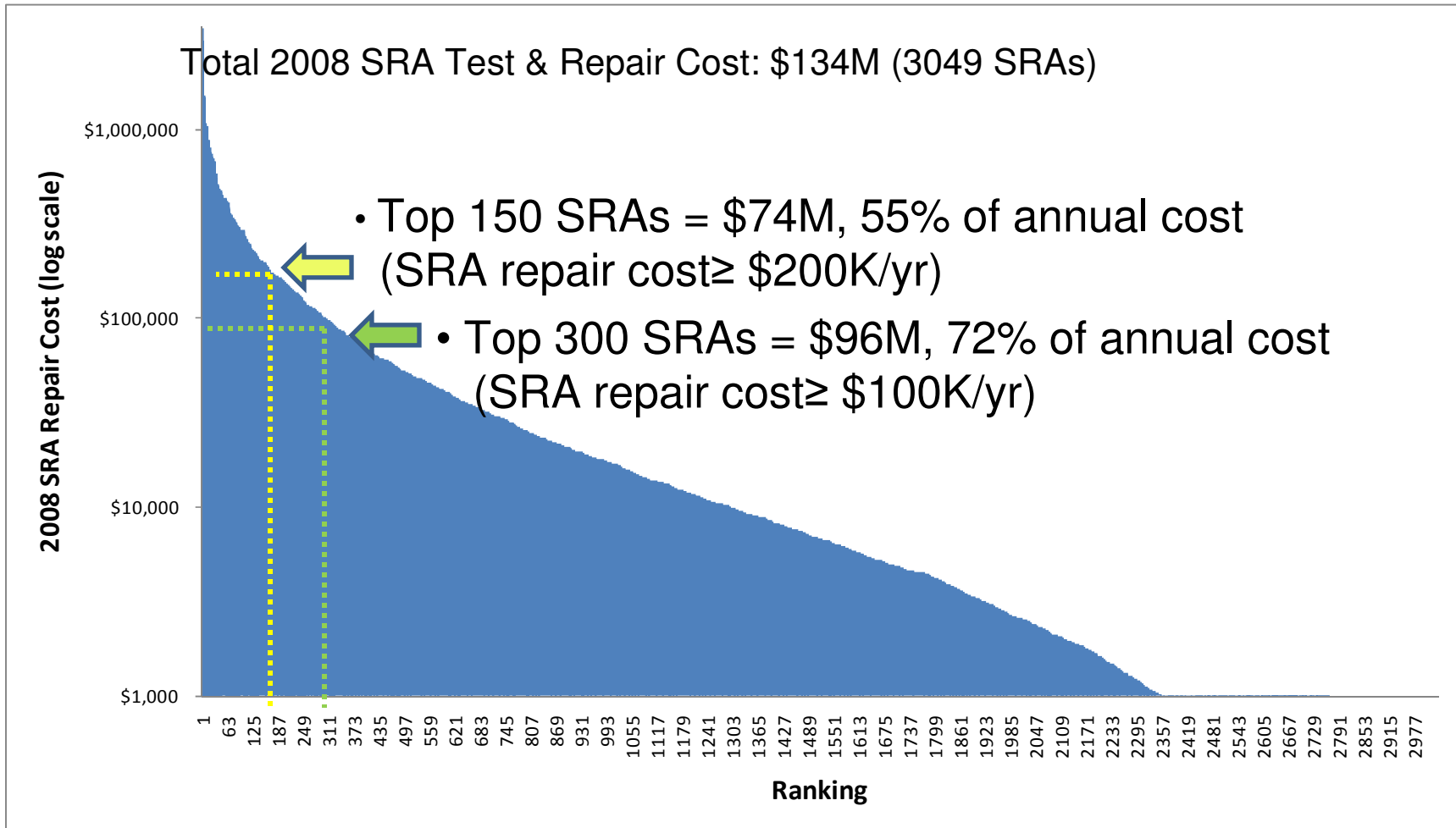


Analyze test and diagnostic effectiveness
Map against known techniques



Recommend cost-effective test improvements

2008 SRA Repair Cost Distribution is Concentrated Across 300 SRAs



Repair Cost is Dominated by BCM1

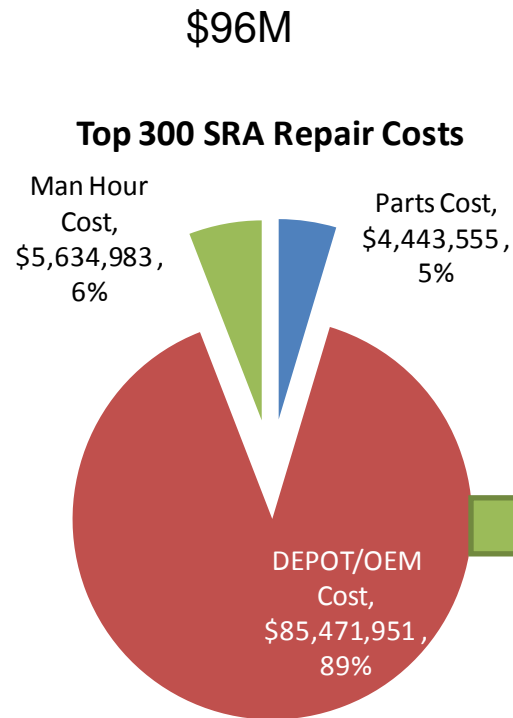


Figure 2. Breakdown showing BCM(Beyond Capability of Maintenance) cost of sending SRAs to Depot/OEM (Source R/S/C, DECPATE)

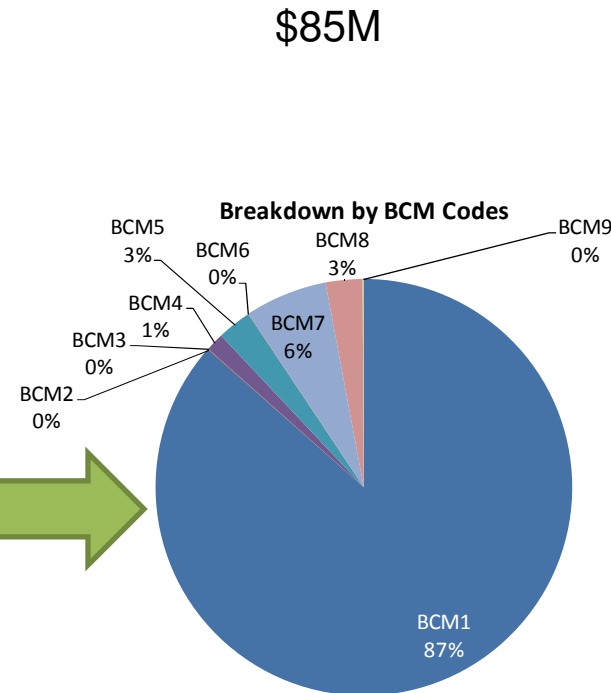
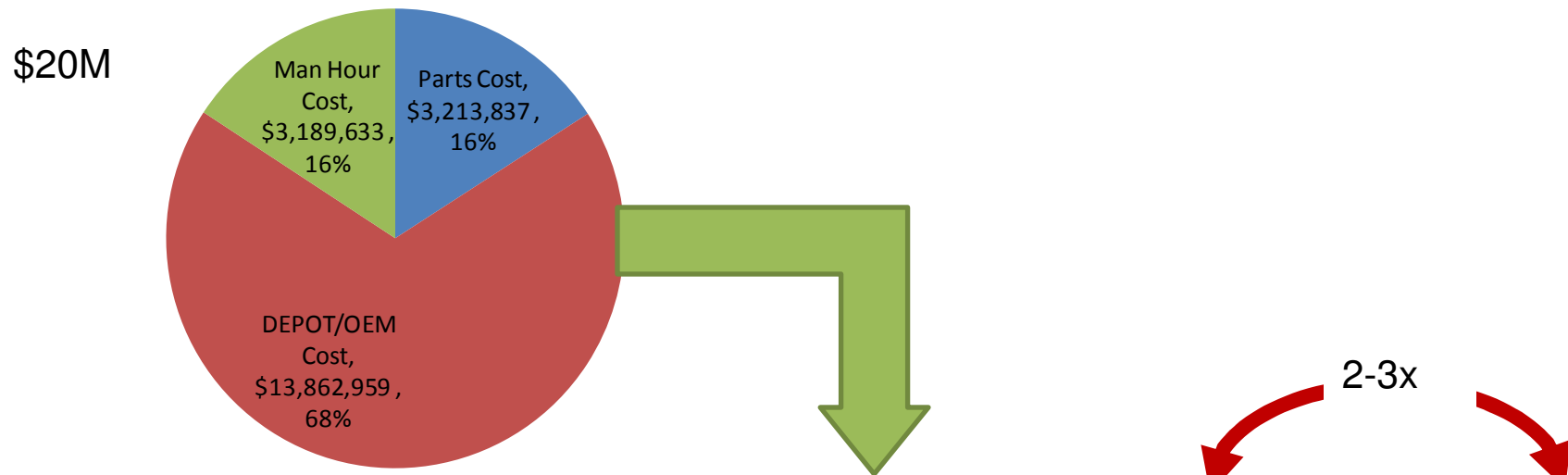


Figure 3. Breakdown showing that the majority are BCM1, “Not Authorized for Repair” (R/S/C, DECPATE, CASS CIP)

- BCM 1 – Repair not Authorized
- BCM 2 – Lack of Equipment, Tools or Facilities
- BCM 3 – Lack of Technical Skills
- BCM 4 – Lack of Parts
- BCM 5 – Fails Test and Check
- BCM 6 – Lack of Technical Data
- BCM 7 – Beyond Authorized Repair Depth
- BCM 8 – Administrative
- BCM 9 - Condemned

BCM Breakdown for SRAs with I-level Test Capability

Subset of top 300 SRAs with I-level Test Capability



	# SRAs	BCMs/ Inductions	BCM %	1	4	5	7	8	BCM Cost	Avg BCM cost	RFI Cost	Avg. RFI cost
All	67	2066/5596	37%						\$13.9M	\$8.6K	\$6.4M	\$3.9K
CASS	44	547/3477	14%	149	63	48	211	64	\$8.2M	\$14.9K	\$4.9M	\$6K
HTS	20	871/1921	45%	529	60	25	189	65	\$5.3M	\$6.1K	\$1.5M	\$1.8K
DLATS/ RADCOM	3	273/294	93%	219			7	6	\$0.4M	\$1.4K	\$0.02M	\$0.9K

Source: R/S/C, DECPATE, CASS CIP

Commercial Test Techniques Considered

SRA Device Technology

	LF analog	Digital	RF
SRA Package Types	BGA	Boundary Scan, Functional	Functional
	SMT	Functional	Functional
	Thru-hole	Nodal impedance, ICT	ICT, Nodal impedance

Commercial Test Techniques Considered

SRA Device Technology

		LF analog	Digital	RF
SRA Package Types	BGA	Functional	Boundary Scan, Functional	Functional
	SMT	Functional	CASS high impact SRAs	Functional
	Thru-hole	Nodal impedance, ICT	ICT, Nodal impedance	Functional

CASS SRA Test Improvement Focus Areas

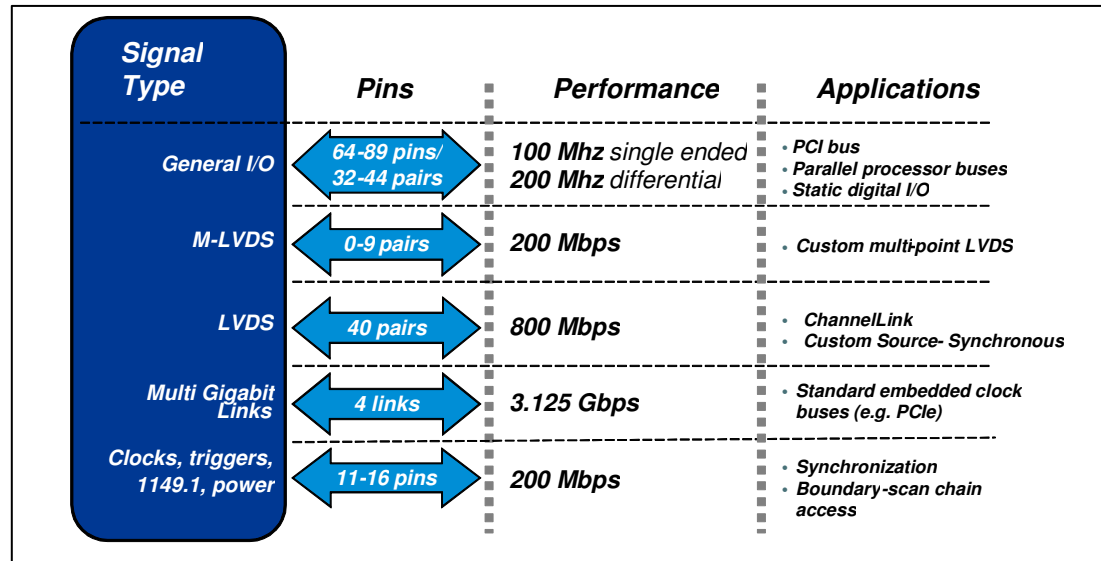
1. **Improve diagnostic resolution:** callouts of up to 10 components
 - Unnecessary replacement of costly, fine pitch ICs
 - 2M (solder shop) damage to the PCB.
2. **Reduce CASS station utilization time**
 - Related to large ambiguity groups, sequential alignment issue, multiple passes required for many SRAs
3. **Streamline alignment process**
 - Interdependent characteristics of many SRA alignments limited by the sequential nature of CASS TPSs
4. **Reduce CND Rates(Can Not Duplicate)**
 - Up to 20% of inductions
 - Radar cards often need to be “matched” at the WRA level
5. **Simplify Interface Device (ID)**
 - Logic level shifters/drivers in the Interface Device (ID)
 - Reduces ID reliability and availability
 - ID issues can be misinterpreted as SRA failures

Improvement Initiatives

Focus Area	PMA 260 Improvement Initiatives
Improve Diagnostic Resolution	<ul style="list-style-type: none"> • <i>ML-PRF-32070 TPS performance specification to tighten ambiguity groups</i> • <i>Incorporate probing into mainstream programming to improve diagnostics:</i> <ul style="list-style-type: none"> • <i>Add Analog/RF Diagnostic Probing for tests with large ambiguity groups</i> • <i>Add Digital Diagnostic Probing to enhance fault dictionary</i> • <i>Funding Phase II SBIR for parallel testing to add a graphical display of multiple simultaneous UUT I/O signals to support technician troubleshooting</i> • <i>Leverage operational test results to improve CASS diagnostics (Smart TPS)</i> • <i>Deploy focused diagnostic tools such as Huntron /Pinpoint where applicable</i>
Reduce Tester Utilization Time	<ul style="list-style-type: none"> • <i>Simplify deployment of parallel test with graphical environment that defines timing relationships across signal types</i>
Streamline Alignment Process	<ul style="list-style-type: none"> • <i>Enhance Real Time Graphics and Measurement to enable interactive alignment</i> • <i>Add analog synchronous stimulus and measurement capability that better emulates system environment to improve test quality</i>
Reduce CND Rates	<ul style="list-style-type: none"> • <i>Improve data collection and analysis for identifying bad actors</i>
Simplify Interface Device	<ul style="list-style-type: none"> • <i>Generic OTPS RFP discourages active fixtures</i> • <i>Proactively evaluating tester requirements for emerging technologies such as video testing, high speed busses that drive use of active IDs</i>

JSF-specific Communications Interfaces

Bus	Application
Custom serial busses	Applications-specific box-to-box
Standard RS busses	General purpose box-to-box
Automotive (MIC, CAN)	Vehicle body control, diagnostics
MIL-STD-1553, H009	Weapons systems and avionics
Discrete digital	Legacy box-to-box signaling
Custom parallel busses	Legacy box-to-box and SRU communication
Standard parallel busses (VME, PCI-33)	SRU-to-SRU for legacy and upgrades
VME2e, VME2eSST, PCI-66	Future SRU-to-SRU communication
Proprietary parallel LVDS	JSF CNI
Proprietary serial LVDS	
StarFabric	JSF EWS backplanes
Channel Link	E2C Radar
Firewire (IEEE-1394B)	JSF Vehicle systems
1 & 2G Fibre Channel	JSF Avionics
Ethernet 10 _{base} X	E2C Main avionics bus
Ethernet 100 _{base} X	E2C Main avionics bus upgrade
4G Fibre Channel	JSF Avionics upgrades
VITA-41, VITA-42, PCI Express, RapidIO	General JSF Computing, signal processing SRU upgrades



JSF Specific Instruments	
JSF-specific Communications Interfaces, including MIC, VAN, 1553, H009, VME, PCI-33, VME2e, VME2eSST, PCI-66, parallel and serial LVDS, StarFabric, Channel Link, Firewire, 1 and 2G Fibre Channel, Ethernet 10 _{base} X, Ethernet 100 _{base} X, 4G Fibre Channel, VITA-41, VITA-42, PCI Express, RapidIO, custom serial busses, customer parallel busses	1
Precision Signal Generator	2
Network Analyzer	1
Spectrum Analyzer	1
Power Meter	1
Vector Generator	1

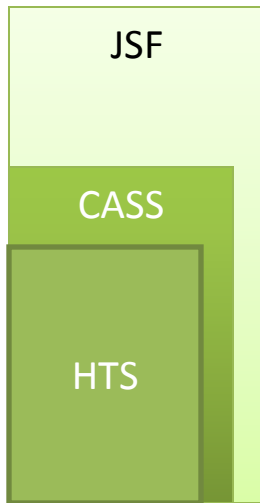
Additional Digital Considerations

- Ability to leverage custom FPGA code
- Flexibility in terms of physical location for handling bus protocols such as PCI that can only travel short distances
- Support of real-time testing
- Boundary Scan Support
 - Maintain design data in case tests need to be regenerated for specific format
 - Must provide high throughput scan pattern generation for FLASH programming or risk exceedingly long test times.

JSF-specific RF Module Test Requirements

- Driven primarily by F-35 AN/APG-81 AESA Radar
- Spectrum Analyzer- up to 44GHz
- Signal Generators- up to 40 GHz
- High Frequency Vector RF Source- up to 20 GHz
- Network Analyzer- up to 44GHz
- Broadband Power Measurement-
 - Only general requirements were identified

SRA Test Configurations Are Supersets



CASS, HTS, JSF SRA Test System Configurations					
Description	HTS 1	HTS 2	CASS 1	CASS 2	JSF
System Core	Qty	Qty	Qty	Qty	Qty
# Racks	1	1	1	1	1
High Power C Size VXI Chassis	1	1	1	1	1
Standard power C size VXI Card Cage	1	1	1	1	1
20 KVA Power Distribution Unit	1	1	1	1	1
Tester CPU (generic PC req'ts)	1	1	1	1	1
CASS compatible dual tier fixture	1	1	1	1	1
Power Supplies and Load					
16V , 20.6 A	4	3	4	4	4
65V, 5.1A	3	3	5	5	5
450V, 2.3A	2	2	3	3	3
140V(rms), 7A(rms)	3	3	3	3	3
500V, 15A, 375 W Load	1	1	1	1	1
Digital Channel Cards					
25 MHz CASS Equivalent Channel Cards	4	4		4	0
50 MHz CASS Equivalent channel Cards			6		6
CASS Equivalent Clock and Sync Capability			1	1	1
CASS equivalent Guided Probe			1	1	1
Low Frequency Analog Instrumentation					
High Accuracy Multi-Function Analog (MFA) Channels Each Channel Includes: • 200 MHz Timer/Counter • 200 MS/s, 14-bit Arbitrary Waveform Generator • 50 MS/s, 12-bit Digitizer	8	8	8	8	1
2-Channel 1 GS/s Digital Oscilloscope	1	1	1	1	1
6.5 Digit DMM	1	1	1	1	1
High Density Multi-Analog Channels (MAC Kit)			3		3
Precision DC Source (Kiethly 2400 or equivalent)	1	1			?
Pulse Generator	2		2	2	2
Synchro/Resolver	2		3		3
Low Frequency Calibrator			1		1
Low Frequency Analog Switching					
Power Switches(>16A)	20	20	20	20	1
1x64 2Amp MUX	1	1	1	1	1
Crosspoint Matrix Chassis	1	1	1	1	1
Port (Input) Module for Instrument Connections	2	2	2	2	2
64 Channel (Output) Module for UUT Connections	4	4	6	4	6
CASS-specific Communication Interfaces					
MIL-STD-1553-A-B (# of ports)			2	2	1
TIA/EIA (RS)-232-C, TIA/EIA (RS)-422-A, TIA/EIA (RS)-485 (# Ports)			2	2	1
JSF Specific Instruments					
JSF-specific Communications Interfaces, including MIC, VAN, 1553, H009, VME, PCI-33, VME2e, VME2eSST, PCI-66, arallel and serial LVDS, StarFabric, Channel Link, Firewire, 1 and 2G Fibre Channel, Ethernet 10baseX, Ethernet 100baseX, 4G Fibre Channel, VITA-41, VITA-42, PCI Express, RapidIO, custom serial busses, customer parallel busses					1
Precision Signal Generator					2
Network Analyzer					1
Spectrum Analyzer					1
Power Meter					1

Conclusion

- 90% of SRA Repair Cost are BCM costs
 - Average BCM Costs are 3x average RFI costs, which may justify forward deployment of certain depot only TPSs
- Implementation of PMA 260 initiatives addresses many of the improvement opportunities identified with current CASS TPSs
- Most high impact TPSs require functional test driven by either device and/or packaging technology.
 - 10 to 30% of these TPS can benefit significantly from diagnostic tools using nodal impedance or ICT. This benefit diminishes as access decreases (because of packaging technology)
- JSF SRAs require significantly higher digital and RF bandwidth
- Parties interested in the survey data should contact Kevin Dusch (kevin.dusch@navy.mil) for a copy