NDIA ATC
Board-Level Test Project

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Agenda

- Project Overview
- Project Volunteers
- Accomplishments
  - Board-Level Test Technologies
  - Candidate Standards/Specifications
  - Evaluation of Standards
- Actions

Board-Level Test Project Overview

- Applicable to all levels of maintenance
- Evaluate the need for additional standards to better facilitate
  - Design-to-test
  - Ease transport of test programs across test systems
  - Leverage data across different board test techniques
- Consider
  - TPS development cost
  - TPS transportability
  - UUT testability
  - Availability of design data
- If additional standards are needed
  - Provide an overview of the recommended standards
  - Provide recommendations for development and publication
- New standards should
  - Maximize the use of commercial specifications and technology
  - Be enforceable
  - Be easy to use
  - Be acceptable to TPS developers

Do we have Standards in place to support Board-Level Test?

Project Volunteers

- Volunteers

Volunteer	Company
Bill Birurakis	Pioneering Decisive Solutions, Inc. (PIDESO)
Bill Byrnes	Teradyne
Bill Curry	Huntron
Bill Kotaska	Boeing
Bill Ross	Navy
Bob Allman	DRS
Bob Augustine	Navy
Bob Fox	Navy
Bill Kotaska	Boeing
Bruce Scott	Lockheed Martin
Dave Droste	DRS
David Carey	Tobyhanna Army Depot
Dean Matsuura	Teradyne
Don Davis	Boeing
Eric Haltiner	Market Access Group Inc.
Kevin Dusch	Navy
Les Orlidge	AAI Corp
Lou Salzano	DME
Mike Dewey	Geotest – Marvin Test Systems Inc.
Mike Frey	Geotest – Marvin Test Systems Inc.
Phil Freeze	DRS
Rick Freeman	Lockheed Martin
Scott Brown - Project Lead	Boeing
Steve Karlovic	CDI
Tim Webb	Diagnosys Systems, Inc.
Tom Farkas	ISI

- To volunteer contact Scott Brown @
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Project Accomplishments

- Identified and Described Board-Level Test Technologies to be Evaluated
  - Each Board-Level Test Technology includes a description of the
    - Information required to use the technology
    - Strengths of the technology
    - Typical challenges using the test technology
  - Selected Board-Level Test Technologies have been further divided to adequately describe the technology
    - For example, Analog Functional Test (RF/uW, Power, Mixed Signal …)
  - Seventeen Board-Level Test Technologies have been identified
- Identified Candidate Standards and Specifications for Evaluation
  - Fifteen candidates identified, ten selected for evaluation
- Identified Evaluation Matrix (Test Technology vs. Standard)
  - One Matrix per Standard

Board-Level Test Technologies

Board Level Test Technology	Information Required to use the Technology	Strengths of Test Technology	Typical Challenges using Test Technology
Analog Nodal Signature Tests	Golden UUT (minimum requirement). CAD Layout files for faster test development.	Quick TP development. Minimal test fixturing. Solid structural test technique. Can be applied with limited or no knowledge of board function. UUT documentation not necessary. UUT is not powered. Basic user training is five days (MTR) Automation can be added.	Structural testing (vs. Functional) - Fault Detection limited to IC's perimeter. Conformal coat must be partially or fully stripped depending on connection method. Developing fault signatures for each component on node to facilitate isolation. Setting tolerances about the V/I curve to ensure functional requirements. Requires component access. Different IC Manufactures may produce different signatures Nodal signature may not reveal specific component failure
Analog In-Circuit Tests	Circuit schematic and board layouts, detailed component information.	Good fault isolation, fairly simple to generate. Best program results if AATG (automatic analog test generation) tool is available - requires minimal knowledge about the UUT and circuitry and assumes ACZ type of measurement system. Unpowered test - minimizes potential damage to UUTs returned from the field.	Test generation becomes difficult if component access is limited. If board is conformally coated, board must be cleaned prior to installing on a fixture. Issues with identifying parallel components - classic challenge is testing bypass capacitors. If DFT rules are not followed, high test coverage could be problematic due to access issues. Does not verify functionality of the UUT - Analog ICT is primarily used for structural / manufacturing fault detection which may limit its use in the repair loop. Typical analog ICT tester resources are limited to stimulus / response in the 100 KHz range-limiting AC measurement of RF components.
Digital In-Circuit Tests (Board Level)	All PLD data. IC structural models. Circuit schematic and board layouts, detailed component information. Board Power requirements	Pseudo-functional testing with potential for excellent fault isolation. Good fault isolation, fairly simple to generate. High Fault coverage Diagnostics to component level Clearly identifies when a component is faulty Program development time	Complex test fixturing. Conformal coat must be stripped. uProcessors difficult to test. Designed to exercise individual ICs - Input to Output testing not practical. Test generation becomes difficult if component access is limited. Detailed component specs aren't always available. Access to BGAs. Testing Monostables or components with a delay
Digital In-Circuit Tests (Component Level - Clip)	Board Power requirements Component Data sheets Board level schematics	Dynamic functional testing with potential for excellent fault isolation. Good fault isolation, fairly simple to generate. High Fault coverage Diagnostics to component level Clearly identifies when a component is faulty. Program development time. Minimal fixture requirements.	Conformal coat must be stripped. uProcessors difficult to test. Board functionality may require NHA for verification. Access to BGAs. Testing Monostables or components with a delay. Detailed component specs aren't always available.
Analog Functional Tests: General Case and baseband signal processing	Schematic, component data sheets, functional requirements. Circuit schematics and detailed data for circuit components. Circuit board design description.	Readily available simulation applications (Spice). Can be applied to most analog circuitry.	Noise can be an issue in the test environment (low level sensor interface). Obtaining functional requirements for all system levels. Fault isolation difficult if component access is limited. Test generation requires an understanding of board function. Detailed component/board data aren't always available.
Analog Functional Tests: RF/Microwave	Schematic, component data sheets, functional requirements. Full performance specs. Cable/connector interface specs. Circuit schematics and detailed data for circuit components. Circuit board design description.	Performance verification with external RF equipment. Can be applied to most analog circuitry.	Requires higher skill set for operators and techs (ie connector torque, instrument familiarity). Some tests can be very subtle (SNR, NF, Return Loss). Obtaining functional requirements for all system levels. Fault isolation difficult if component access is limited. Test generation requires an understanding of board function. Detailed component/board data aren't always available.
Analog Functional Tests: Mixed-Signal	Schematic, component data sheets, functional requirements. Some digital to analog timing design data (settling time etc.). Circuit schematics and detailed data for circuit components. Circuit board design description.	Complete functional test possible; more "system-like" testing. Readily available simulation applications (Spice). Can be applied to most analog circuitry.	Requires both Analog and Digital stimuli as well as synchronization between domains. Obtaining functional requirements for all system levels. Fault isolation difficult if component access is limited. Test generation requires an understanding of board function. Detailed component/board data aren't always available.
Analog Functional Tests: Power	Schematic, component data sheets, functional requirements. Operational cooling requirements. Specs on pulsed operation. Circuit schematics and detailed data for circuit components. Circuit board design description.	Some problems only occur under power conditions (thermal, breakdown, EMI etc.). Readily available simulation applications (Spice). Can be applied to most analog circuitry.	Cooling of UUT during Testing. Possible hazardous scenarios (ie High Voltage, Burns, UUT self destruction) . Obtaining functional requirements for all system levels. Fault isolation difficult if component access is limited. Test generation requires an understanding of board function. Detailed component/board data aren't always available.

Board-Level Test Technologies

Board Level Test Technology	Information Required to use the Technology	Strengths of Test Technology	Typical Challenges using Test Technology
Digital Functional Tests - Edge Connector	All PLD data. IC structural models. Schematic, component data sheets, Circuit schematics and detailed data for circuit components. Circuit board design description. Board Power Requirements	Readily available simulation applications (LASAR). Can be applied to most digital circuitry.	Requires sophisticated, dynamic digital test instrumentation. Fault isolation difficult if component access is limited. Test generation requires an understanding of board function. Detailed component/board data aren't always available.
Boundary Scan	Schematic Vendor BSDL files.	High fault coverage Becoming more useful as component density increases and access to component pins decreases.	Potential technique only if UUT designed with Boundary Scan Any "non-scannable" devices are problematic if access is not provided via other means.
Flying Probes - Single head	Golden UUT. CAD Layout files preferred. Board pc trace, component layout & CAD data	For CCA testing - full visibility to all modes. Automatic test generation, good test coverage. Documented 10 to 1 productivity increase over manual probing.	Conformal coating removal. BGA or fine pitch packaging and board coatings make access difficult. Manual test development is time consuming.
Flying Probes - Two heads	Golden UUT. CAD Layout files preferred. Board pc trace, component layout & CAD data	For CCA testing - full visibility to all modes Node to node test capability. Gold Disk compatible for ASA test.	Conformal coating removal BGA or fine pitch packaging and board coatings make access difficult. Manual test development is time consuming
Flying Probes - Multi-head (3+)	Golden UUT. CAD Layout data required in most cases. Board pc trace, component layout & CAD data	For CCA testing - full visibility to all modes. Node to node test capability. Gold Disk compatible for ASA test. Can be implemneted with In-circuit test methods.	Conformal coating removal BGA or fine pitch packaging and board coatings make access difficult. Manual test development is not possible in most cases.
Optical Test	Board pc trace and component layout	Detecting manufacturing defects Detects component marking, orientation …	Only detects physical defects.
X-Ray Tests	Board pc trace and component layout	Detecting manufacturing defects Detects hidden defects.	Only detects physical defects.
Vibration Tests	Board pc trace and component layout	Detecting manufacturing defects	Only detects physical defects.
Thermal Imaging Tests	Thermal map of good board.	Fast test time	Subjective unless image processing and AI are used.

Candidate Standards/Specifications

Standard	Title	Status	Applicability Comments	Review
IEEE Std 1149.1	Test Access Port and Boundary Scan Architecture	Reaffirmed 2008 (4-year cycle)	Definitely a test technology for board-level and chip level diagnostics of digital circuits	Y
IEEE Std 1149.4	Mixed-Signal Test Bus	Pub 1/1/2000, Active Project	Extends "dot 1" to include analog	N
IEEE Std 1149.6	Boundary Scan Testing of Advanced Digital Networks	Pub 1/1/2003 (no Re-affirm or project noted)	Same as 1149.1 with additional of ac-coupled digital and hi-speed differential networks are facilitated.	N
IEEE Std 1445	Digital Test Interchange Format (DTIF)	Re-affirmed 2004, re-affirmation in progress	Very active, supported standard for testing of digital circuit cards	Y
IEEE Guide 1546	Digital test interchange format (DTIF) application	Active	Active, supported Guide to the use of 1445 DTIF	Y
IEEE Std 1671.1	Draft Trial-Use Standard for Automatic Test Markup Language (ATML) for Exchanging Automatic Test Equipment and Test Information via XML, Exchanging Test Descriptions	In Ballot	Supports transportibility of TPSs for either SRUs or LRUs to other ATE system by a common data format for test descriptions.	Y
IEEE Std 1671.3	Draft Trial-Use Standard for Standard Automatic Test Markup Language (ATML) for Exchanging Automatic Test Information via XML (Xtensible Markup Language): Exchanging UUT (Unit-Under-Test) Description Information	Active, Pub 2008	Supports configuration and identification of characteristcs of the UUT (SRU, LRU, Etc.). Provides a common data format for information.	Y
IEEE Std 1636.1	Trial-Use Standard for Software Interface for Maintenance Information Collection and Analysis (SIMICA): Exchanging Test Results and Session Information via the eXtensible Markup Language (XML)	Active, Pub 2008	Common data format for test results to be able to compare tests at different maintenance levels and testers. Note that the base standard 1636 is also applicable, but isn't ATML/XML-based.	Y
Mil-Hdbk-2165	DEPARTMENT OF DEFENSE TESTABILITY PROGRAM FOR SYSTEMS AND EQUIPMENTS	Active, Pub July 1995	This standard prescribes a uniform approach to testability program planning, establishment of diagnostic concepts and testability (including BIT) requirements, testability and test design and assessment, and requirements for conducting testability program review	Y
MIL-STD-334	DEPARTMENT OF DEFENSE STANDARD PRACTICE: DISPLAYED MESSAGES FOR AUTOMATIC TEST EQUIPMENT	Active, Pub 2006	Sets uniform requirements for written or graphical information delivered to users of automatic test equipment (ATE) by computer-controlled output devices. Standardized messages and abbreviations minimize confusion in any testing (SRUs or LRUs).	N
MIL-HDBK-2084	DEPARTMENT OF DEFENSE HANDBOOK FOR MAINTAINABILITY OF AVIONICS AND ELECTRONIC SYSTEMS AND EQUIPMENT	Active, Pub July 1995	Covers the common maintainability design requirements to be used in military specifications for avionic and electronic systems and equipment. Includes topics sim-to 2165 for Test Points, BIT, FMECA, physical aspects supporting Maintainability.	Y
MIL-STD-2076	MILITARY STANDARD, UNIT UNDER TEST (UUT)COMPATIBILITY WITH AUTOMATIC TEST EQUIPMENT (ATE), GENERAL REQUIREMENTS FOR	Active?, Pub March 1978	This Standard presents the design requirements for a UUT which will make it compatible for test on an ATE. Thus designed, the UUT will possess the attributes necessary to maximize the benefits possible through use of ATE and minimize the cost necessary to achieve those benefits.	N
MIL-PRF-32070	NAVAIR Generic OTPS RFP	Aug '09	"Red Team Package"	Y
	Gold Disk Specification		Addresses pinpoint & Huntron technology	Y

Evaluation of Standards

Board Level Test Technology	Design to Test	Ease of Transport across test systems	Leverage Data across test techniques
Analog Nodal Signature Tests			
Analog In-Circuit Tests			
Digital In-Circuit Tests (Board Level)			
Digital In-Circuit Tests (Component Level - Clip)			
Analog Functional Tests: General Case and baseband signal processing			
Analog Functional Tests: RF/Microwave			
Analog Functional Tests: Mixed-Signal			
Analog Functional Tests: Power			
Digital Functional Tests - Edge Connector			
Boundary Scan			
Flying Probes - Single head			
Flying Probes - Two heads			
Flying Probes - Multi-head (3+)			
Optical Test			
X-Ray Tests			
Vibration Tests			
Thermal Imaging Tests			

One Worksheet per Standard

Actions

- Near Term Actions
  - Identify Potential Commercial Standards
  - Evaluate the Standards and Specifications with respect to
    - Design to Test, Transportability, Leverage Data across test techniques
- Project Completion
  - First Quarter 2010

Backup

AUTOMATIC TEST SYSTEMS EXECUTIVE DIRECTORATE
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9 February 2009

From: DoD ATS Executive Directorate
To: Chairman, National Defense Industrial Association Automatic Testing Committee

Subj: Request for Study and Recommendations Relative to Board-Level Test

1. Many different approaches to board-level test are currently in use in both government and industry. These include shorts test, analog nodal signature analysis, analog in-circuit test, digital in-circuit test, analog functional test, digital functional test, boundary scan, use of flying probers, optical test, x-ray test, vibration, and thermal imaging. Effective board test may require a combination of these approaches.

2. It is requested that the NDIA ATC conduct a study of the various approaches to board-level test and provide a recommendation to the DoD ATS Executive Directorate relative to the need for additional standards to better facilitate design-to-test, to ease transport of test programs across test systems, and to leverage data across different board test techniques. The study should review standards and specifications currently applicable to board-level test at all levels of maintenance from factory through intermediate level. If it is determined that additional standards are needed, request provide an overview of the applicability of each of the recommended standards, and a recommendation for the working group or organization which should undertake development and publication of the standard. Consider the impact on TPS development cost, TPS transportability, UUT testability and the availability of design data. Any recommended new standard should maximize the use of commercial specifications and technology, be enforceable, be easy to use and be generally acceptable to TPS developers.

3. Please direct questions to the undersigned at (301) 757-6907 (e-mail william.ross@navy.mil).

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