

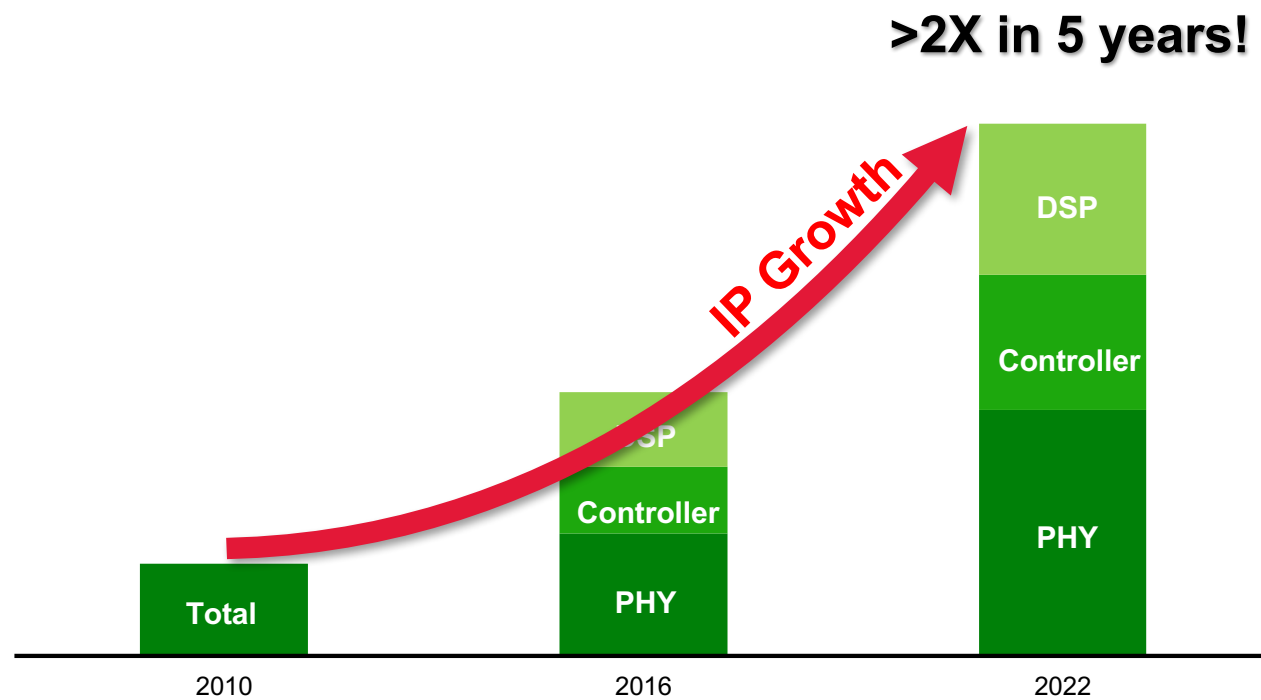


NDIA Panel Discussion

Dino Bekis, Vice President Marketing, IP Group
Trusted Microelectronics Workshop
February 2, 2017

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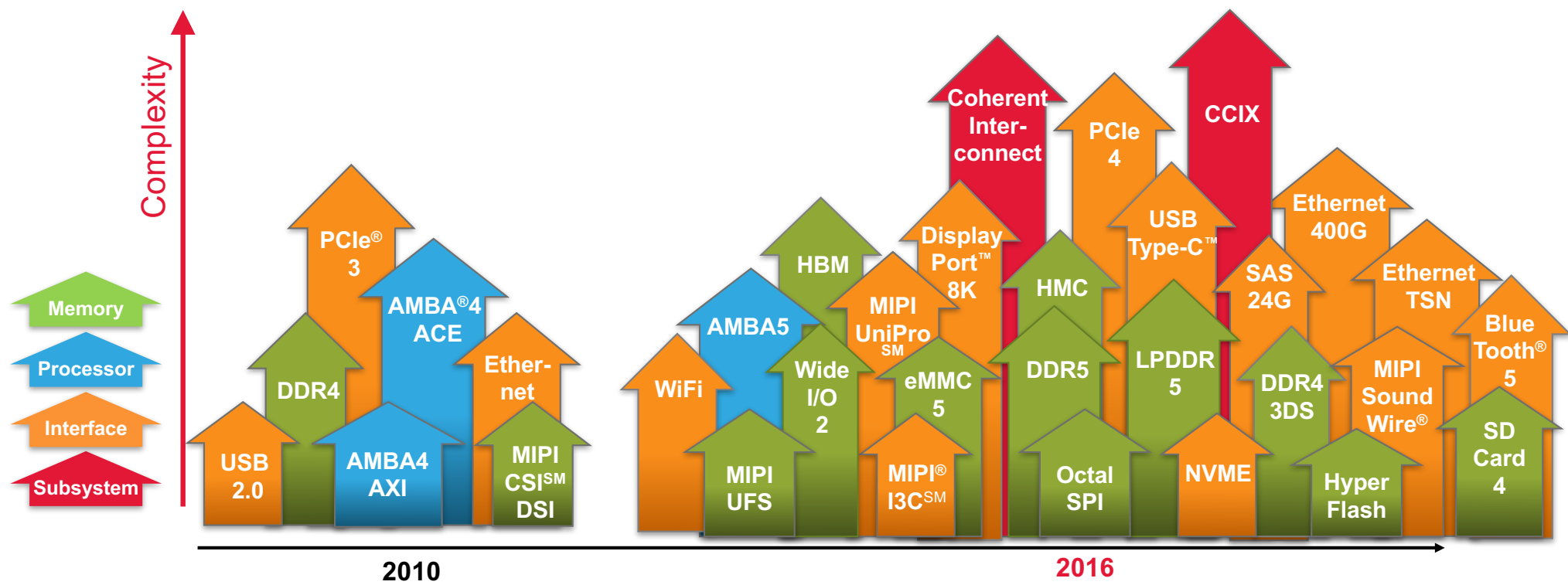
Commercial IP Market Is Dramatically Expanding



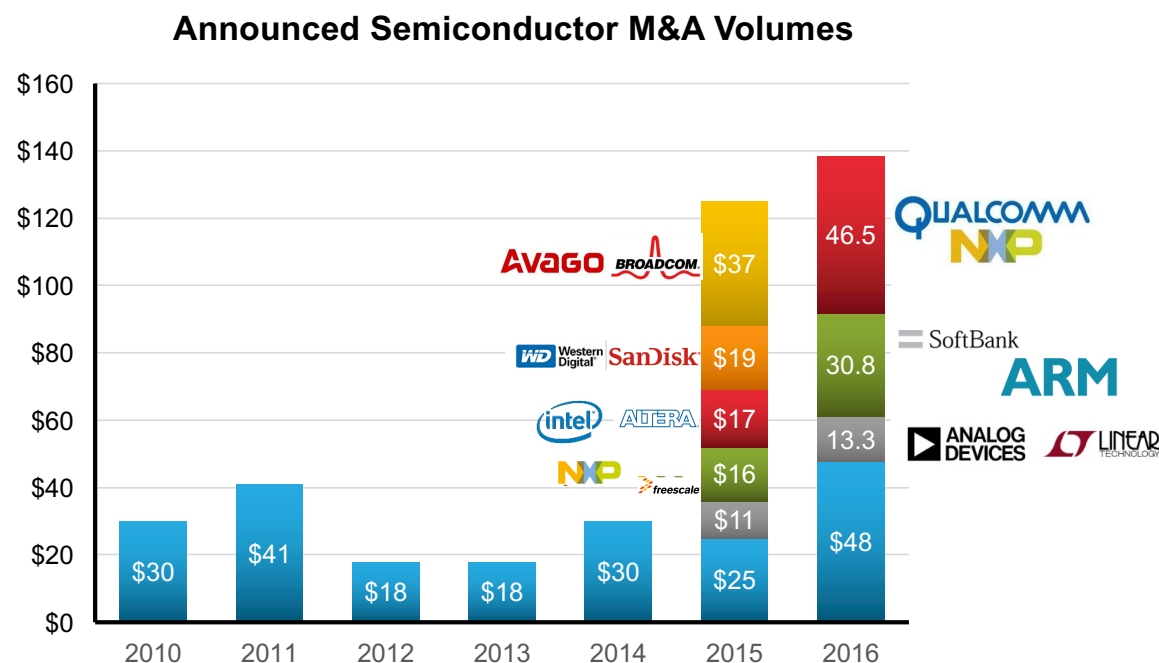
Sources: Press Releases, Magazines, Investor Presentations, Scientific Journals, Expert Interviews, and Market Analysis

New Standard Protocols Fuel Demand

More complex, shorter life, narrower markets



Consolidation Creates Expanding Need



M&A Objectives:

- Reduced OPEX
- Accelerated TTM
- Greater innovation

Commercial IP aligns with M&A objectives

Source: Semiconductor Engineering <http://semiengineering.com/the-urge-to-merge/> - Tom Stokes, Evercore, an investment banking advisory firm

Business Imperatives for Commercial IP

- Focus limited engineering resources on differentiating technology
 - Apply most valuable resources on highest value-add content
 - Expand technical capabilities beyond current staff, improve OPEX leverage
- Access to new technologies with reduced first-adopter risks
 - Silicon-proven technology in leading-edge nodes
 - Deep engagement and leadership with standards bodies
- Faster time-to-market
 - Established software ecosystem
 - 3rd-party IP integration experience
- Leverage the knowledge of 100s of customers, 1000s of designs
 - Multiple markets exposure, broad interoperability
 - Production-hardened, trusted solution

Five Pillars of Security



Confidentiality

- Protection against access secret data/code via encryption

Integrity

- Protection against modification of data/code/system state

Authentication

- Protection against forged identity in illegal communication or operation

Access Control

- Protection against unauthorized usage of resource or operation

Availability

- Protection against malicious depletion of resource from normal usage

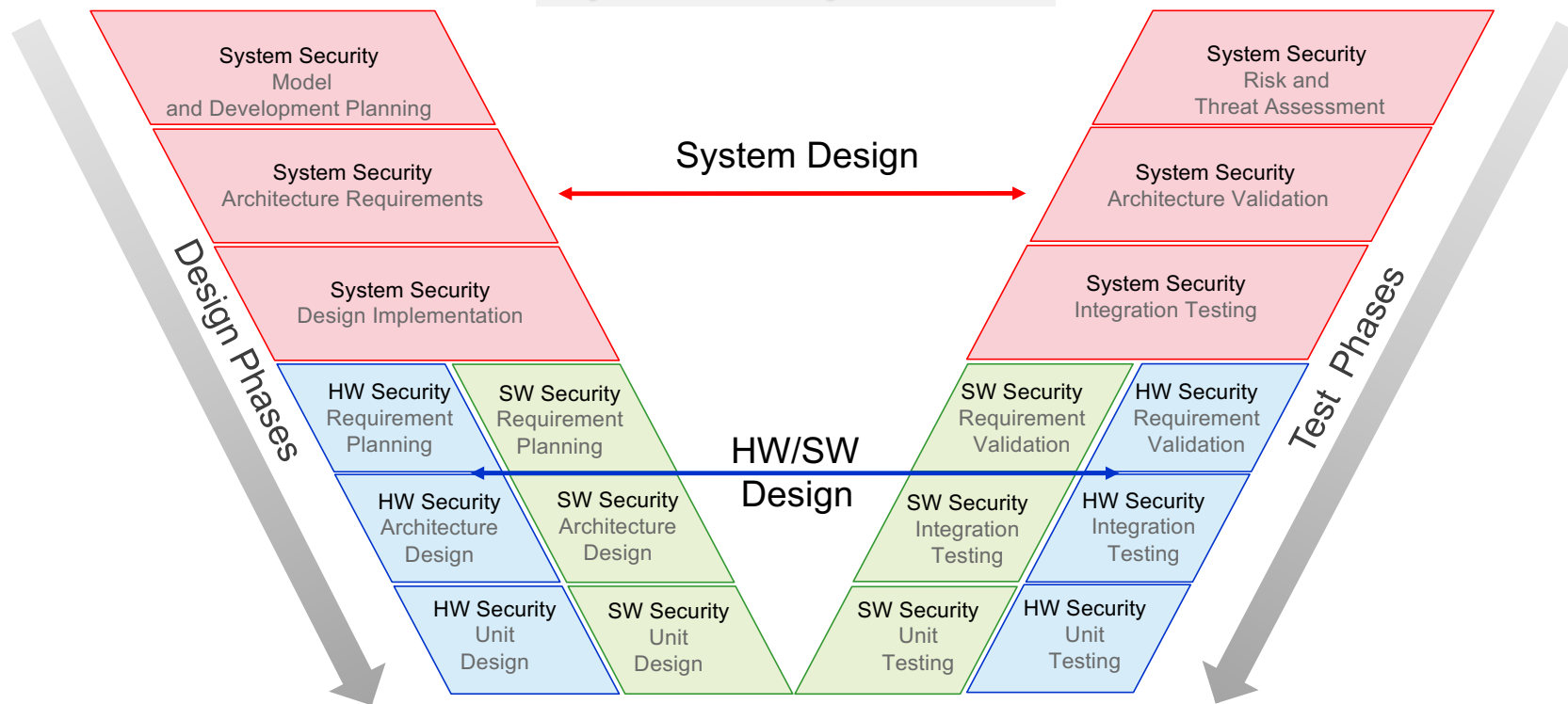
Emerging Needs and Challenges for Secure Silicon

- Secure software engineering process well established in tier-1 companies
 - e.g., Microsoft SDL
- Some segments have established practice due to regulation
 - e.g., smartcard/POS for finance/payment, Common Criteria
- Demand in industry segments handling mission/safety-critical tasks
 - e.g. IoT infrastructure, automotive, aerospace
- No pan-industry standard practice for silicon development
 - Broad range of metric-driven signoff
 - Deeper cycles, high value bugs, increasingly large designs

Combined Security and Safety in Automotive

Secure engineering process similar to ISO 26262 functional safety

Cybersecurity V-Model



SAE J3061 defines security practice V-model similar to ISO 26262 model on safety

Secure Semiconductor Products

Secure silicon = hardware + software + process

Secure Silicon

Secure Hardware IP

Secure Software IP

Secure Engineering Process

Secure
CPU

Crypto
HW

RNG
OTP

Platform
HW

Crypto
API
Library

Secure
Protocol
Stack

Secure
OS

Secure
Dev
Tools

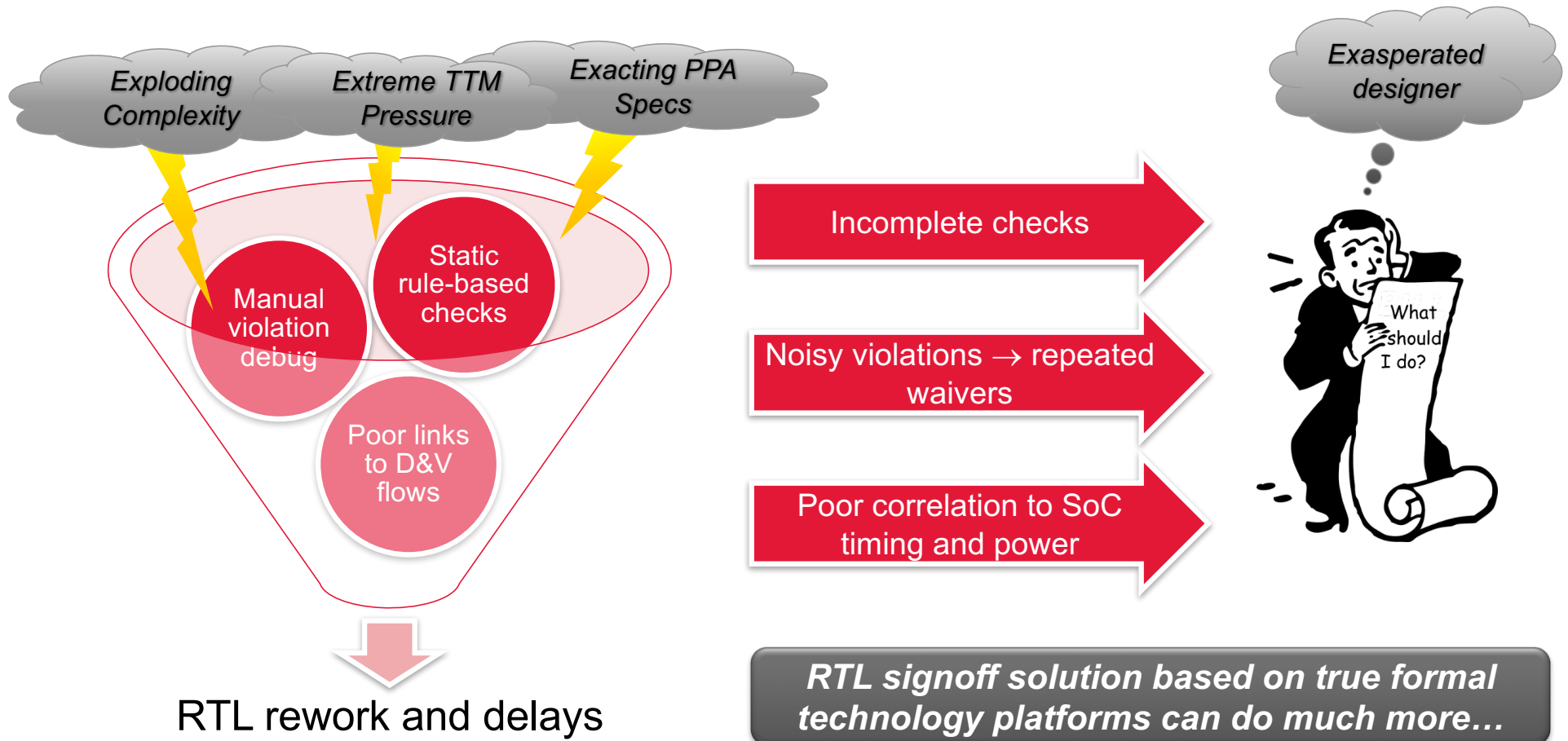
Threat
Models

Security
Risk
Assess-
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Security
Testing

Security
Review

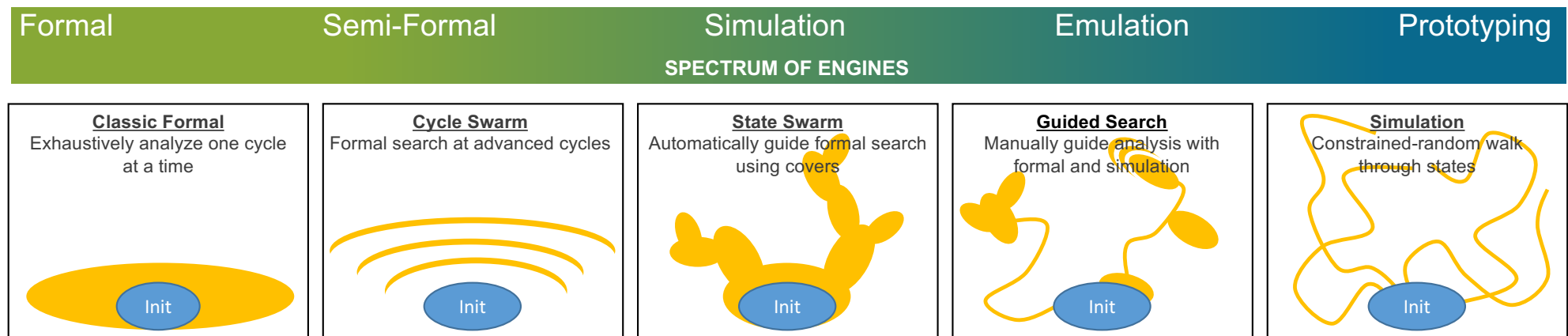
Many RTL Signoff Solutions Lack Formal Intelligence



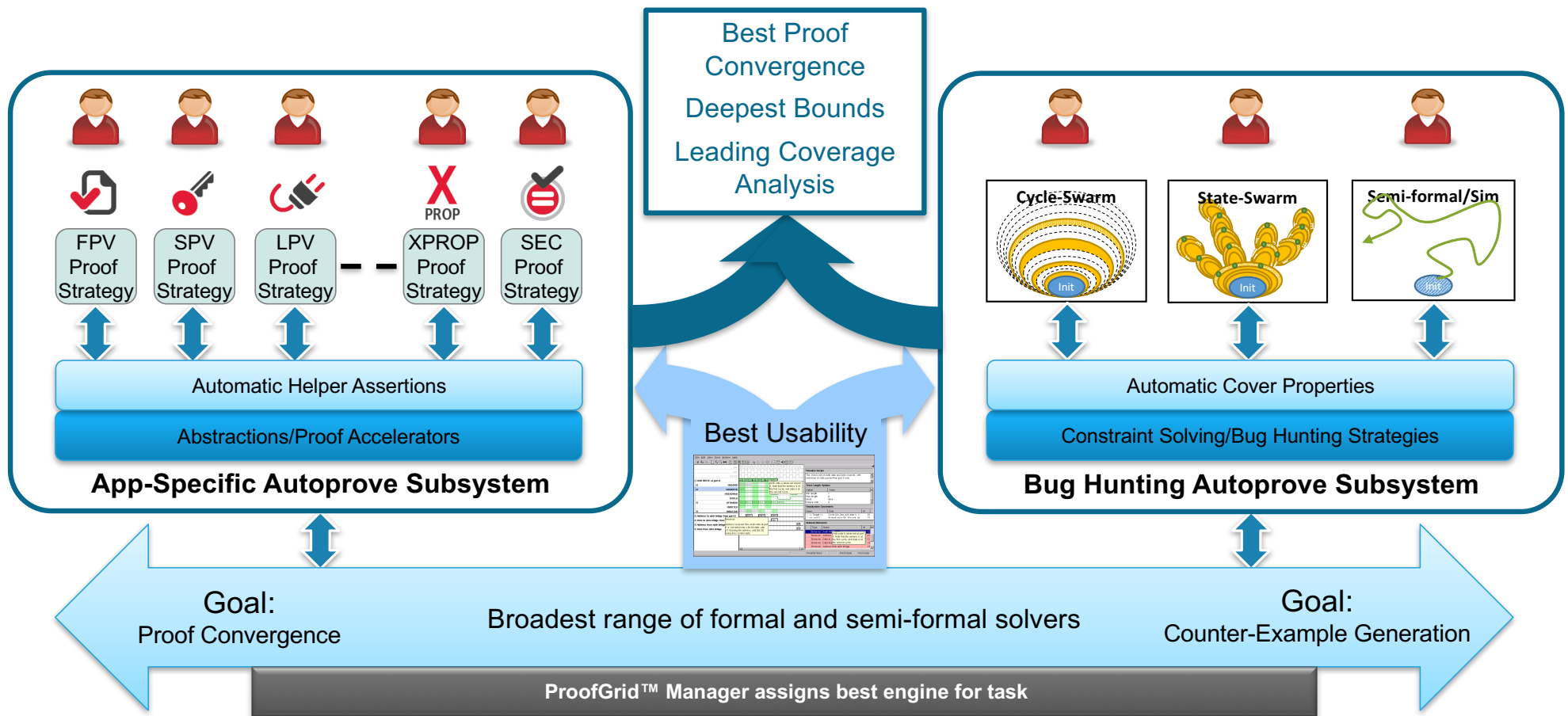
Trusted, Assured, Secured

Towards a comprehensive, practical solution

- **Interrelated requirements**
 - Evolving threat vectors
 - No silver bullet
 - Requires coordinated orchestration of multiple methods
- **Cadence: Rich set of foundational assets**
 - Algorithms, heuristics
 - Tools, flows
 - Experience, expertise
- **Innovation progression**
 - Analysis methods
 - Metrics
 - Transformations
 - Optimizations

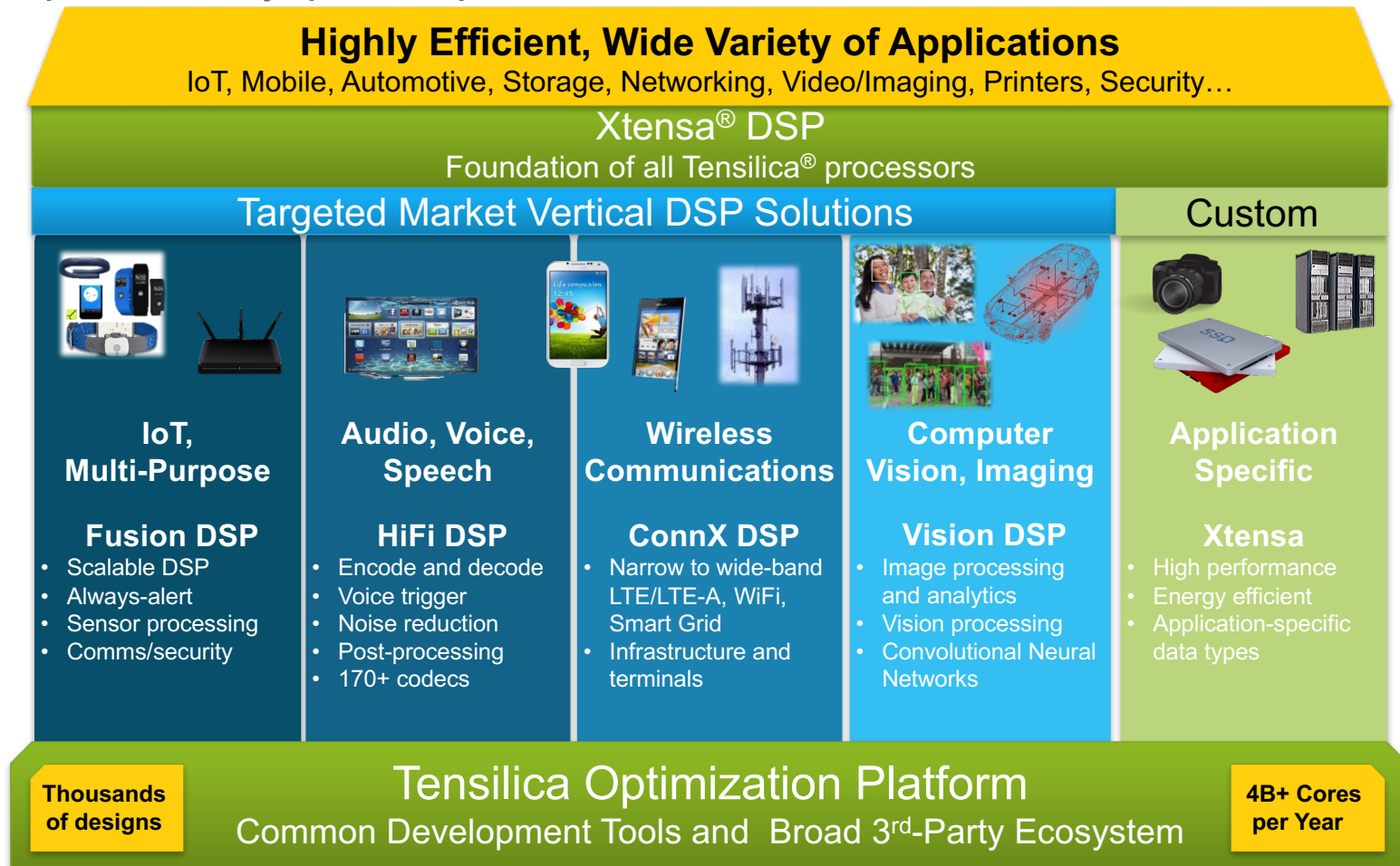


JasperGold Apps: Ease-of-Use, High Capacity, and Performance



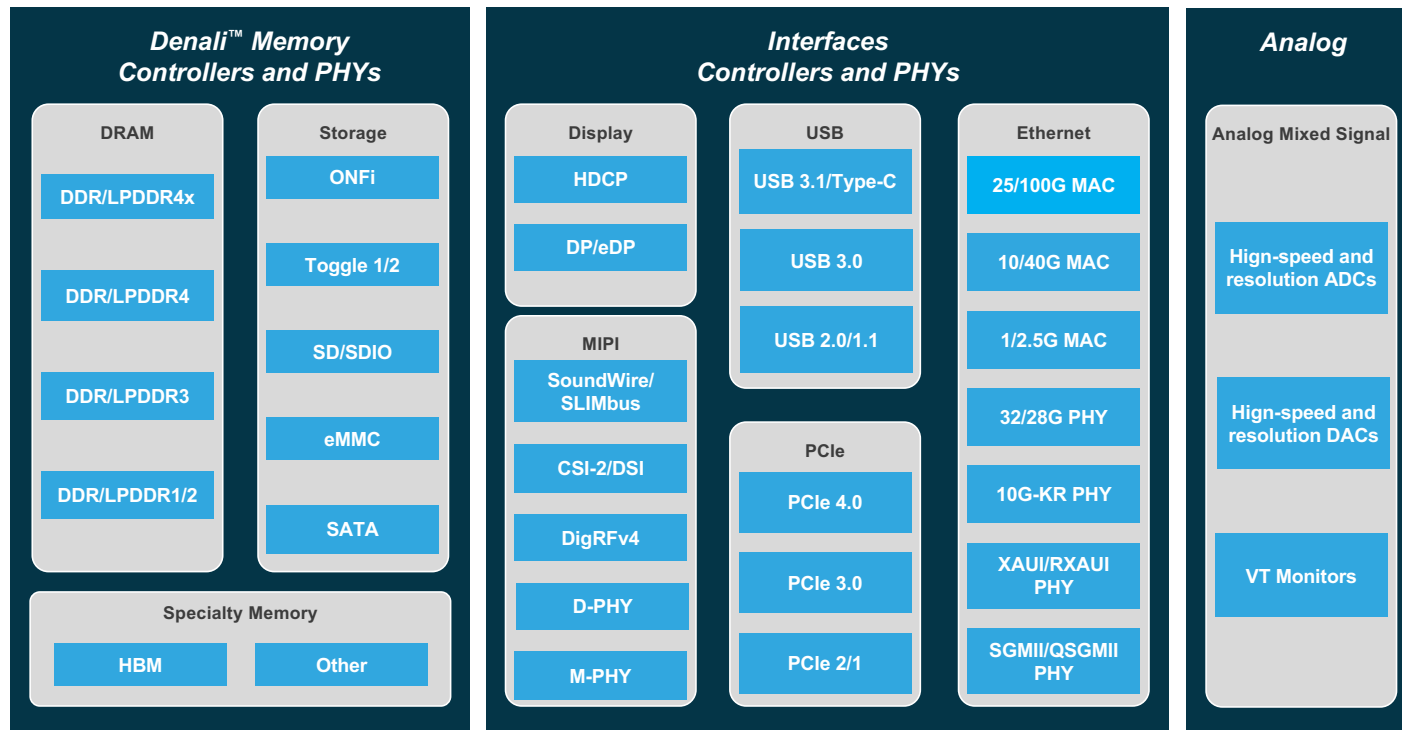
Tensilica Processor IP

Leadership scalability, power, performance, and area



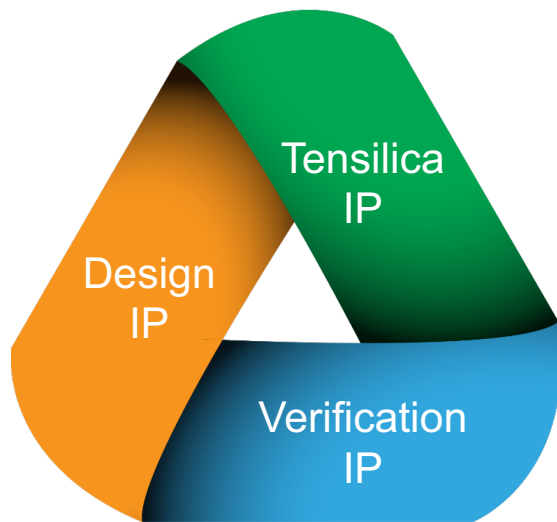
Cadence Design IP Portfolio

Broad and growing set of solutions for your next SoC



Cadence IP – Build the Future Faster

Unleashing your creativity to architect, integrate, and verify leading-edge SoCs



Faster time to market,
highly differentiated products

- CNN-, vision-, and audio-optimized solutions
- Low-power embedded DSP platform
- Rapid, verified generation/configuration

- Latest protocol IP, including DDR, PCIe
- Silicon proven in the most popular process nodes
- High quality through multi-dimensional verification

- Consistently first to market with the right protocols
- Complete and comprehensive tools
- Work with any language or methodology



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